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ANALOG COMMUNICATIONS

LAB MANUAL

EC-351

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BAPATLA ENGINEERING COLLEGE: : BAPATLA

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EC 351 ANALOG COMMUNICATIONS LAB

NOTE: A minimum of 10(Ten) experiments have to be performed and recorded by the candidate to attain eligibility for University Practical Examination

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1. VOLTAGE SHUNT FEED BACK AMPLIFIER

AIM: To design a voltage shunt feed back amplifier using transistor and to find the effect of feedback on bandwidth and voltage graph

APPARATUS:

1.Transistor_(BC547)

2. Resistors- 1k,68k,8.2k.lOOΩ,220Ω, 5.6k

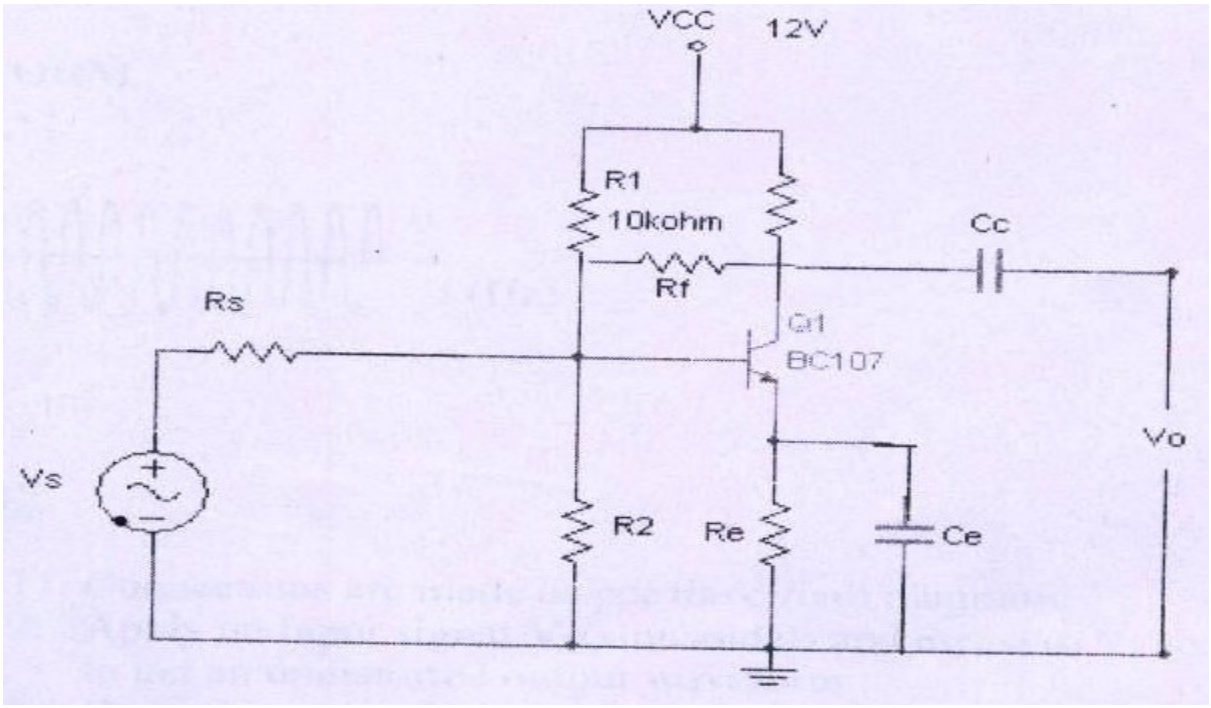
3. Capacitors _47μF,100μF.

4.Function Generator

5.RPS Unit

6.CRO 7-Connecting probes

CIRCUIT DIAGRAM:



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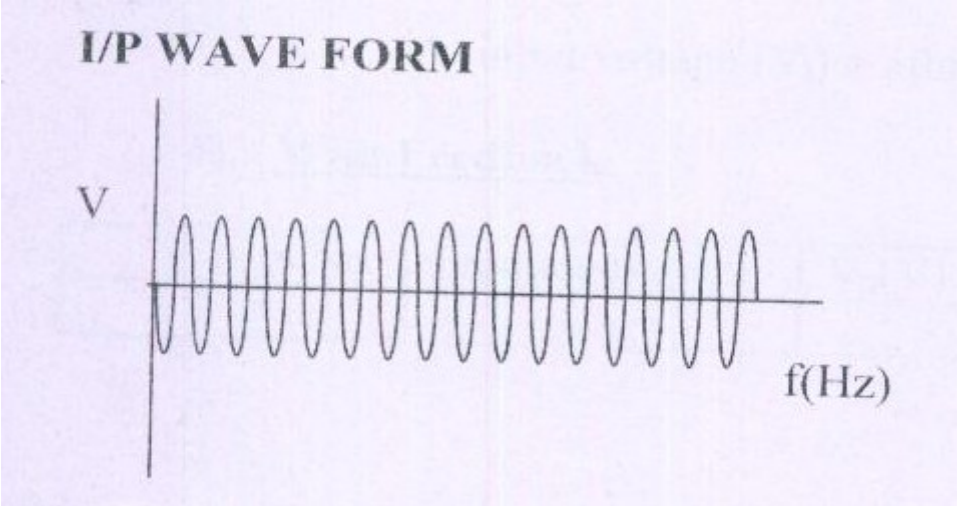
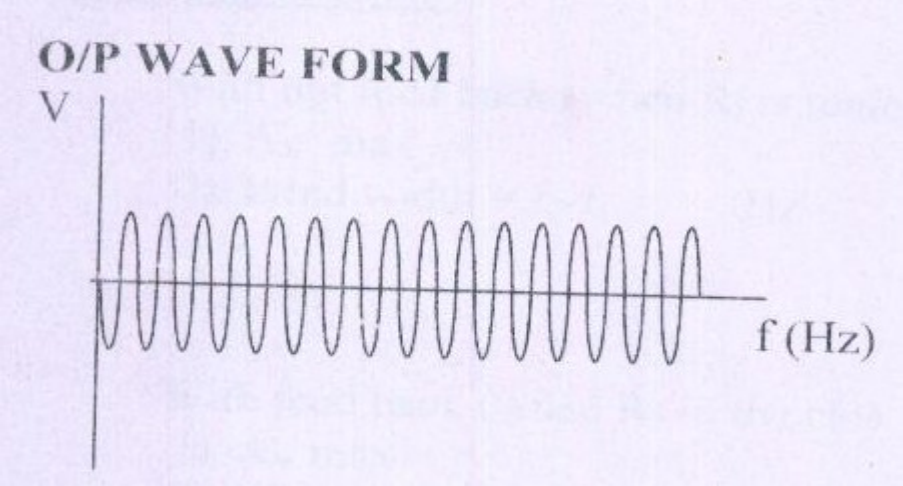
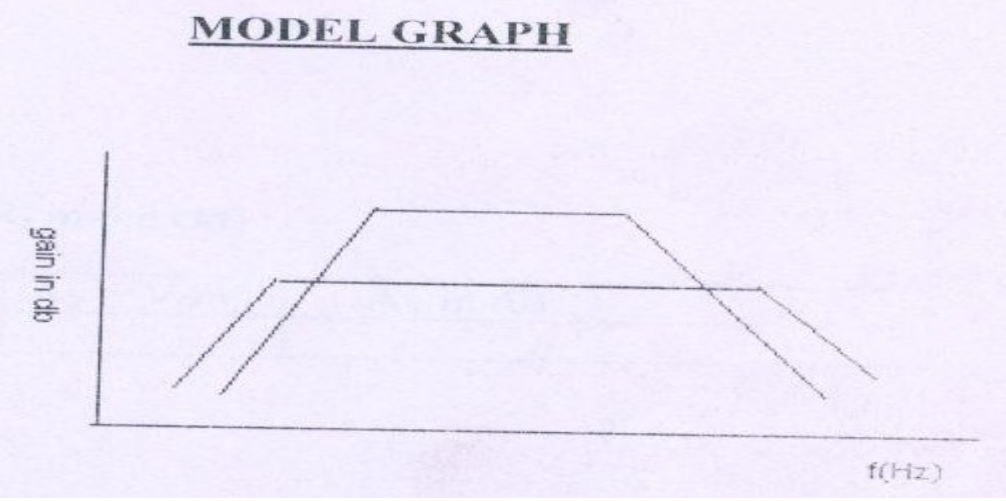
MODEL WAVE FORMS







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PROCEDURE:

1. Connections are made as per the circuit diagram.
2. Apply an input signal V_s (sinusoidal) and measure V_i to be min value to get an undistorted output waveform .
3. By keeping V_i to be constant value and vary its frequency such that note down the corresponding output! Signal's amplitude and tabulate them.
4. Calculate the voltage gain in Db.
5. By removing the feed back resistor (R_f) in the amplifier ckt .repeal [lie above procedure.
6. Now plot the graphs for gain in dB Vs frequency and calculate the-maximum gain bandwidth with feedback & with out feedback *and* compare the values

OBSERVATION:

At input voltage (V_i) = 50mV **With Feedback**

Sl.No.	Frequency (Hz)	Vo(V)	Av=Vo/Vi	Av in dB

With out Feedback (by removing Rr in the circuit)

Sl.No.	Frequency (Hz)	Vo(V)	Av=Vo/Vi	Av in dB

CALCULATIONS:

With out feed back (when R_f is removed) & With feed back (when R_f in the ckt)

1) Av max =

2) Band width = $f_2 - f_1$ = Hz

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Result:

2. Amplitude Modulation & Demodulation

Aim: 1. To generate amplitude modulated wave and determine the percentage modulation.

2. To Demodulate the modulated wave using envelope detector.

Apparatus Required:

Name of the Component/Equipment	Specifications/Range	Quantity
Transistor(BC 107)	f_T = 300 MHz P_d = 1W I_c(max) = 100 mA	1
Diode(0A79)	Max Current 35mA	1
Resistors	1KΩ, 2KΩ, 6.8KΩ, 10KΩ	1 each
Capacitor	0.01μF	1
Inductor	130mH	1
CRO	20MHz	1
Function Generator	1MHz	2
Regulated Power Supply	0-30V, 1A	1

Theory:

Amplitude Modulation is defined as a process in which the amplitude of the carrier wave c(t) is varied linearly with the instantaneous amplitude of the message signal m(t).The standard form of an amplitude modulated (AM) wave is defined by

$$s(t) = A_c[1 + K_a m(t)\cos(2\pi f_c t)]$$

Where K_a is a constant called the amplitude sensitivity of the modulator.

The demodulation circuit is used to recover the message signal from the incoming AM wave at the receiver. An envelope detector is a simple and yet highly effective

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device that is well suited for the demodulation of AM wave, for which the percentage modulation is less than 100%.Ideally, an envelop detector produces an output signal that follows the envelop of the input signal wave form exactly; hence, the name. Some version of this circuit is used in almost all commercial AM radio receivers.

The Modulation Index is defined as, m = $\frac{(E_{max} - E_{min})}{(E_{max} + E_{min})}$

Where E_{max} and E_{min} are the maximum and minimum amplitudes of the modulated wave.

Circuit Diagrams:

For modulation:

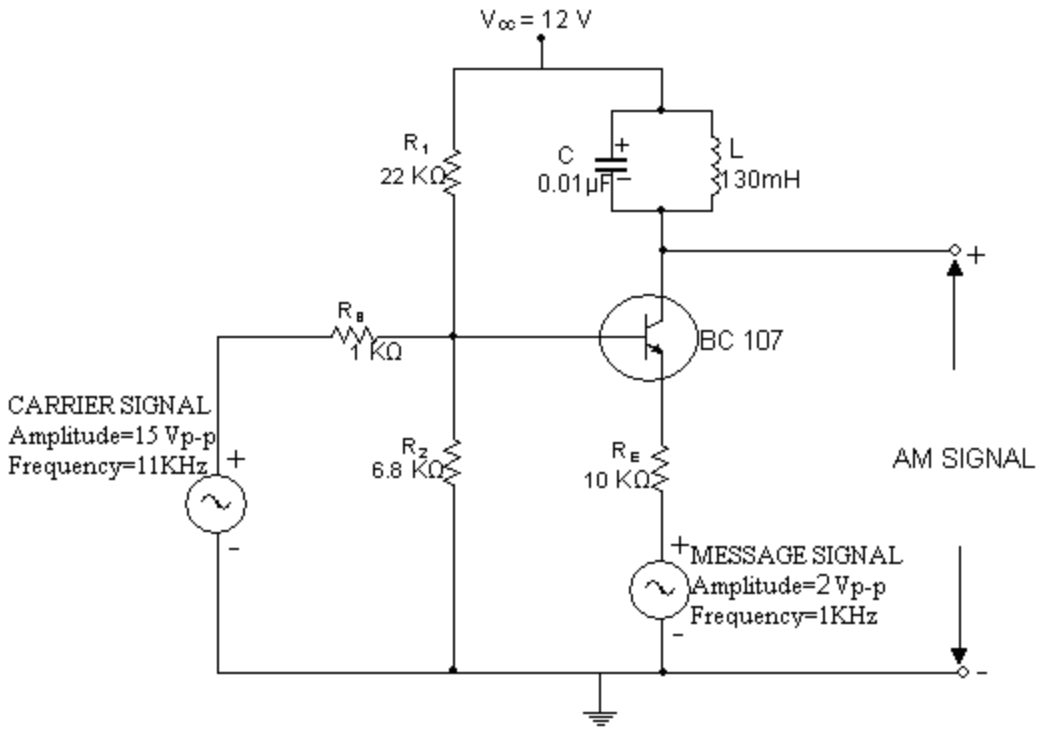

Fig.1. AM modulator

For demodulation:

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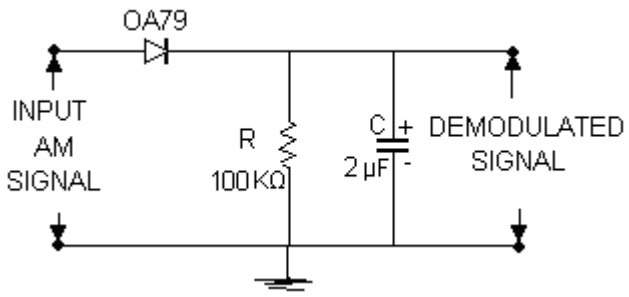

Fig.2. AM demodulator

Procedure:

1. The circuit is connected as per the circuit diagram shown in Fig.1.
2. Switch on + 12 volts V_{CC} supply.
3. Apply sinusoidal signal of 1 KHz frequency and amplitude 2 Vp-p as modulating signal, and carrier signal of frequency 11 KHz and amplitude 15 Vp-p.
4. Now slowly increase the amplitude of the modulating signal up to 7V and note down values of E_{max} and E_{min}.
5. Calculate modulation index using equation
6. Repeat step 5 by varying frequency of the modulating signal.
7. Plot the graphs: Modulation index vs Amplitude & Frequency
8. Find the value of R from $f_m = \frac{1}{2\pi RC}$ taking C = 0.01μF
9. Connect the circuit diagram as shown in Fig.2.
10. Feed the AM wave to the demodulator circuit and observe the output
11. Note down frequency and amplitude of the demodulated output waveform.
12. Draw the demodulated wave form .,m=1

Sample readings:

Table 1: f_m= 1KHz, f_c=11KHz, A_c=15 V p-p.

S.No.	V_m(Volts)	E_{max}(volts)	E_{min} (Volts)	m	%m (m x100)

Table 2: A_m= 4 Vp-p f_c =11KHz, A_c=15 V p-p.

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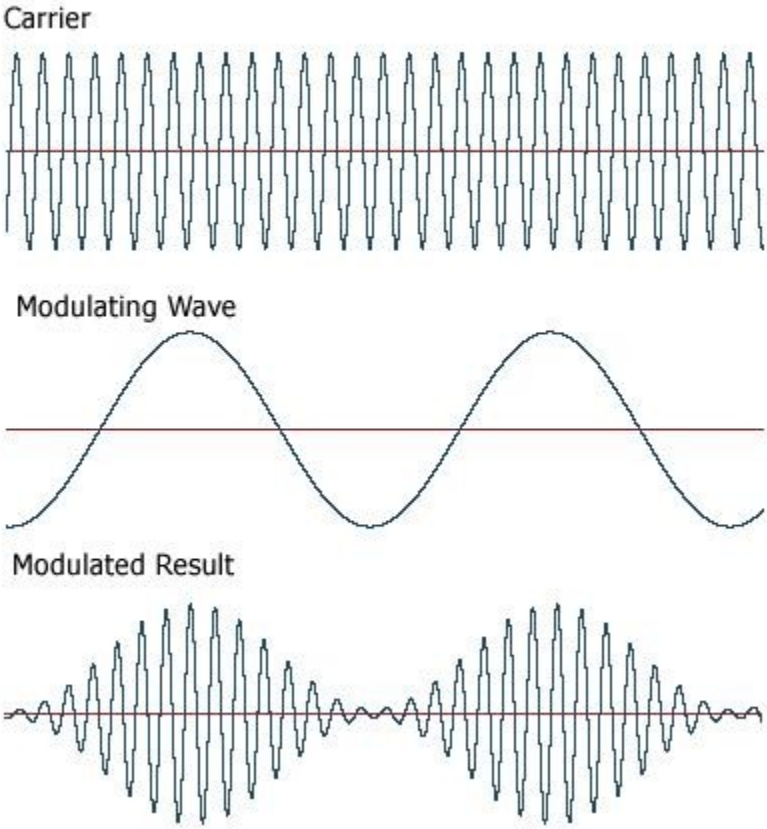
S.No.	f_m(KHz)	E_{max}(volts)	E_{min}(Volts)	m	%m (m x100)

Waveforms and graphs:



Precautions:

1. Check the connections before giving the power supply
2. Observations should be done carefully.

3. CLASS-A POWER AMPLIFIER

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Aim: Design a class-A inductor coupled power amplifier to deliver 4W power to 10 Ohms load resistor.

Apparatus:

S.No	Name of the Component /equipment	Specifications	Qty
1	Power transistor (BD139)	V_{CE} =60V, V_{BE} = 100V I_C = 100mA h_{fe} = 40 to160	1
2	Resistor (designed values)	Power rating=0.5w Carbon type	4
3	Capacitors(designed values)	Electrolytic type Voltage rating= 1.6v	3
4	Function Generator	0 -1MHZ	1
5	Cathode Ray Oscilloscope	20MHZ	1
6	Regulated Power Supply	0-30V,1Amp	1
7	Inductor(designed values)	Operating temperature=ambient	1

Theory: The power amplifier is said to be class A amplifier if the Q point is selected in such a way that output signal is obtained for a full input cycle. For class A power amplifier position of Q point is at the centre of mid point of load line. For all values of input signals the transistor remains in the active region and never enters into the cut off or saturation region. When an ac signal is applied, the collector current flows for 360^0 of the input cycle. In other words, the angle of collector current flow is 360^0 i.e... One full cycle. Here signal is faithfully reproduced at the output without any distortion. This is an important feature of class A operation. The efficiency of class A operation is very low with resistive load and is 25%. This can be increased to 50% by using inductive load. In the present experiment inductive load is used.

Circuit Diagram:

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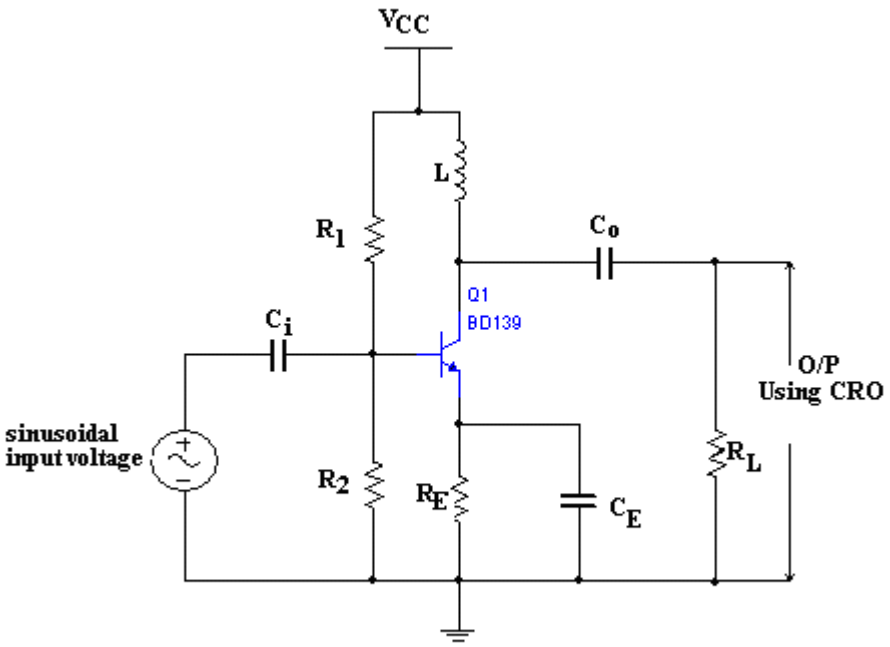

Design Equations:

Given data: R_L= 10Ω, $P_{L\,max}$= 4W, f=1KHZ

1) Selection of L:

$\omega L >> R_L$

$L >> R_L/2\pi f_L$ = 10/6.28(1K) = 1.59mH

2) Selection of V_{CC}:

The maximum power which can be delivered is obtained for $V_m = V_{CC}$

(if v_{min}=0)

$P_{L\,max} \leq V_{CC}^2 / 2R_L$

$V_{CC}^2 \geq P_{Lmax} \times 2R_L$

V_{CC} = 8.94V

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3) Selection of R_E:

$I_{CQ} = (P_{C\,max}/R_L)^{1/2} = (12.5/10)^{1/2} = 1.118A$

$I_{CQ}=V_{CC}/(R_{ac}+R_{dc})$ where $R_{ac}= R_L$, $R_{dc}= R_E$

$I_{CQ}=V_{CC}/(R_L+R_E)$, $R_E = (V_{CC}/I_{CQ}) - R_L$, $R_E = 2\Omega$

4) Selection of biasing resisters R_1 & R_2:

$V_{BB}= V_{BE}+V_E$

$V_E = I_{CQ}*R_E = 2.24V$

$V_{BB}= 0.6+2.24 = 2.84V$

The voltage across R_2 is

$V_{BB}=V_{CC}R_2/(R_1+R_2)$

$2.84 = 8.94R_2/(R_1+R_2) \Rightarrow R_2 = 0.465\ R_1$

$R_B = R_1R_2/(R_1+R_2)$

⇨ $R_1 = 50.4\Omega$, $R_2 = 23.4\Omega$

Capacitor calculations:

To provide low reactances almost short circuit at the operating frequency

f=1KHZ. $X_{CE} = 0.01R_E$, $Xc_i = 0.1\ R_B$, $Xc_0 = 0.1\ R_L$

5) Selection of C_E:

$Xc_E = R_E/100$ $C_E = 7.95mF$

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6) Selection of C_i& C_0:

$Xc_i \approx R_B/10 = 1.6\Omega$

$C_i = 99\mu F$

7) $Xc_0 \approx R_L/10 = 1\Omega$ $C_0 = 0.159mF$

Procedure:

1. Connect the circuit as shown figure and supply the required DC voltage

2. Feed an AC signal at the input and keep the frequency at1 KHZ and amplitude 5V.Connect a power o/p meter at the o/p.

3. Change the o/p impedance in steps for each value of impedance and note down the o/p power.

4. Plot a graph between o/p power and load impedance. From this graph find the impedance for which the o/p power is maximum. This is the value of optimum load.

5. Select load impedance which is equal to 0V or near about the optimum load. See the wave form of the o/p of the C.R.O.

6. Calculate the power sensitivity at a maximum power o/p using the relation.

Power sensitivity = output power / (rms value of the signal)^2

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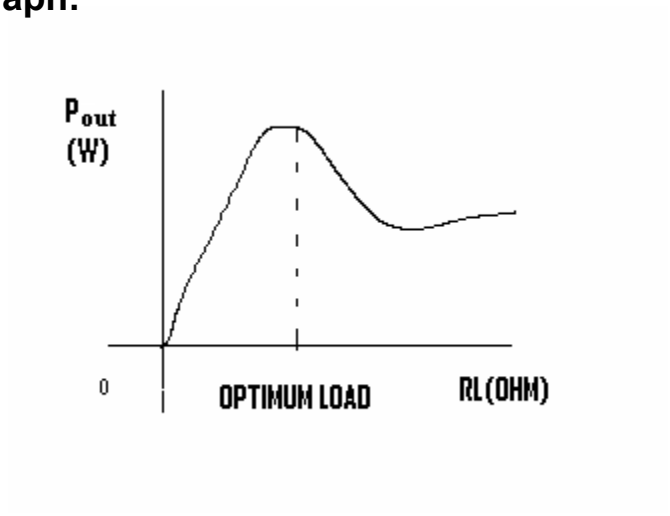
Tabular Form:

S.No	R_L(Ohm)	D.C Input Power P_{in} (W)	A.C output Power P_{out} (W)	η=(Pac)/(Pdc)*100

Model Graph:



Precautions:

1. Connections should be done care fully.
2. Take the readings with out any parallax error.

Result: Simulation and practical results of class A power amplifier are observed.

4. RC PHASE SHIFT OSCILLATOR

Aim: To determine the frequency of oscillations of an RC Phase shift oscillator.

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Apparatus Required:

S. No	Name of the Component/Equipment	Specifications	Quantity
1	Transistor(BC107)	I_{cmax}=100mA P_D=300mw V_{ceo}=45V V_{beo}=50V	1
2	Resistors - 56KΩ,2.2KΩ,100KΩ,10KΩ	Power rating=0.5w Carbon type	1 3
3	Capacitors 10μF/25V ,0.01μF	Electrolytic type Voltage rating=1.6v	2 3
4	Potentiometer	0-10KΩ	1
5	Regulated Power Supply	0-30V,1A	1
6	Cathode Ray Oscilloscope	20 MHz	1

Theory:

In the RC phase shift oscillator, the combination RC provides self-bias for the amplifier. The phase of the signal at the input gets reverse biased when it is amplified by the amplifier. The output of amplifier goes to a feedback network consists of three identical RC sections. Each RC section provides a phase shift of 60^0. Thus a total of 180^0 phase shift is provided by the feedback network. The output of this circuit is in the same phase as the input to the amplifier. The frequency of oscillations is given by

$F=1/2\pi RC (6+4K)^{1/2}$ Where, $R_1=R_2=R_3=R$,

$C_1=C_2=C_3=C$ and

$K=R_C/R$.

Circuit Diagram:

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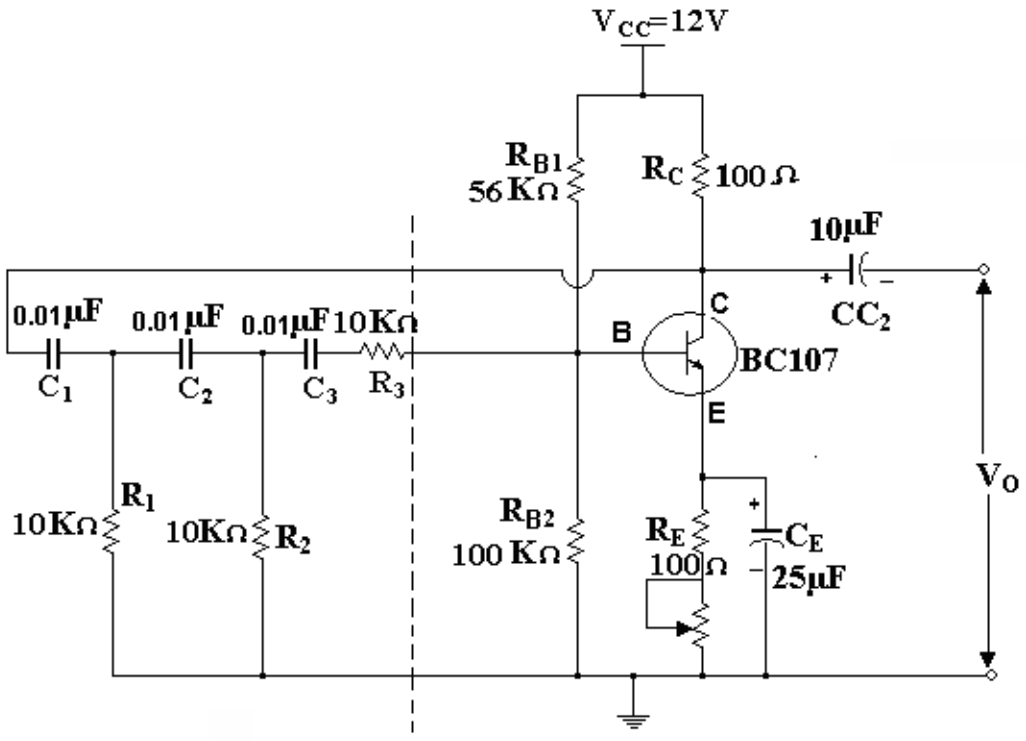

Fig A. RC Phase shift Oscillator

Procedure:

1. Connect the circuit as shown in Fig A.
2. Switch on the power supply.
3. Connect the CRO at the output of the circuit.
4. Adjust the R_E to get undistorted waveform.
5. Measure the Amplitude and Frequency.
6. Compare the theoretical and practical values.
7. Plot the graph amplitude versus frequency

Theoretical Values:

$f = 1 / 2 \pi RC \sqrt{6+4K}$

$=1 / 2 \pi (10K) (0.01\mu F) \sqrt{6+4(0.01)}$

$= 647.59Hz$

Tabular Form:

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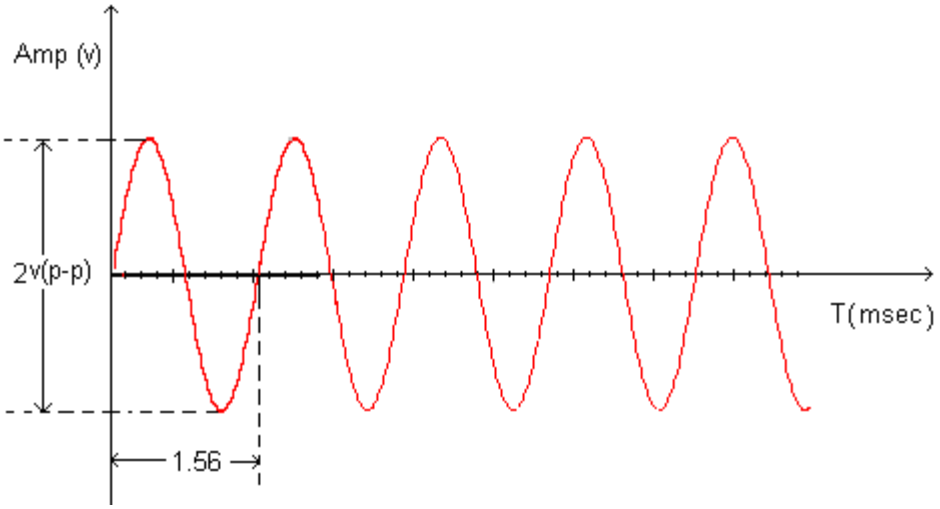
S.NO	Theoretical Frequency(Hz)	Practical Frequency(Hz)	% Error

Model Graph:



Result:

The frequency of RC Phase Shift Oscillator is determined.

5(a). HARTLEY OSCILLATOR

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Aim:

To design a Hartley oscillator and to measure the frequency of oscillations.

Apparatus Required:

S.No	Name of the Component/Equipment	Specifications	Quantity
1.	Hartley Oscillator Circuit Board	___	1
2.	Cathode Ray Oscilloscope	20MHz	1
3.	Decade Inductance Boxes	___	2

Theory:

In the Hartley oscillator shown in Fig A. Z_1, and Z_2 are inductors and Z_3 is an capacitor. The resistors R and R_2 and R_E provide the necessary DC bias to the transistor. C_E is a bypass capacitor C_{C1} and C_{C2} are coupling capacitors. The feedback network consisting of inductors L_1 and L_2 , Capacitor C determine the frequency of the oscillator.

When the supply voltage $+V_{cc}$ is switched ON, a transient current is produced in the tank circuit, and consequently damped harmonic oscillations are setup in the circuit. The current in tank circuit produces AC voltages across L_1 and L_2 . As terminal 3 is earthed, it will be at zero potential.

If terminal is at positive potential with respect to 3 at any instant, then terminal 2 will be at negative potential with respect to 3 at the same instant. Thus the phase difference between the terminals 1 and 2 is always 180^0. In the CE mode, the transistor provides the phase difference of 180^0 between the input and output. Therefore the total phase shift is 360^0. The frequency of oscillations is

$f = 1/2\pi\sqrt{LC}$ where $L= L_1 + L_2$.

Circuit Diagram:-

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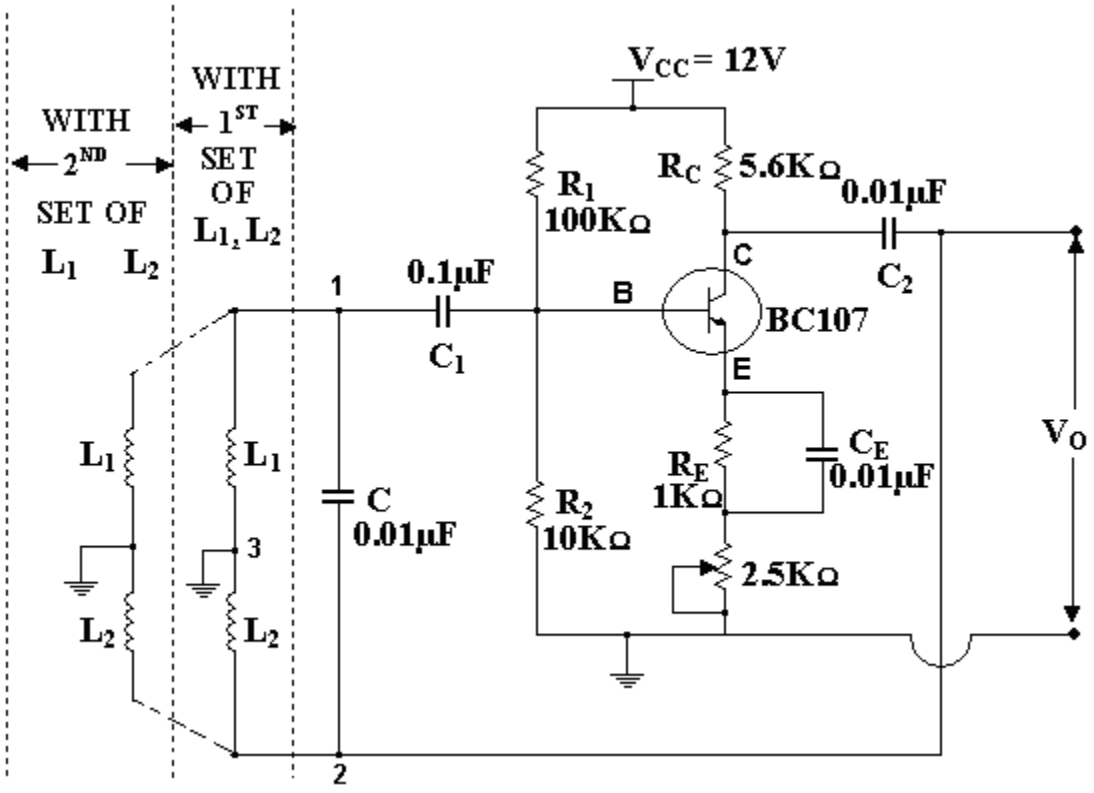

Fig A: Hartley oscillator

Procedure:

1. Switch on the power supply by inserting the power card in AC mains.
2. Connect one pair of inductors as L_1 and L_2 as shown in the dotted lines of Fig A.
3. Observe the output of the oscillator on a CRO, adjust the potentiometer R_E on the front panel until we get an undistorted output. Note down the repetition period (T) of observed signal. Compute $f_O = 1/T$ (R_E can adjust the gain of the amplifier).
4. Calculate the theoretical frequency of the circuit using the formulae.
5. Repeat the steps 2 to 4 for the second pair of inductors L_1 and L_2 .Tabulate the results as below.

Tabular Form:

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S.No	Condition	Frequency , f_o (KHz)		% Error
		Practical	Theoretical	
1	$L_1 = L_2 = 100mH$		3.558	
2	$L_1 = L_2 = 50mH$		5.032	

Model Graph:

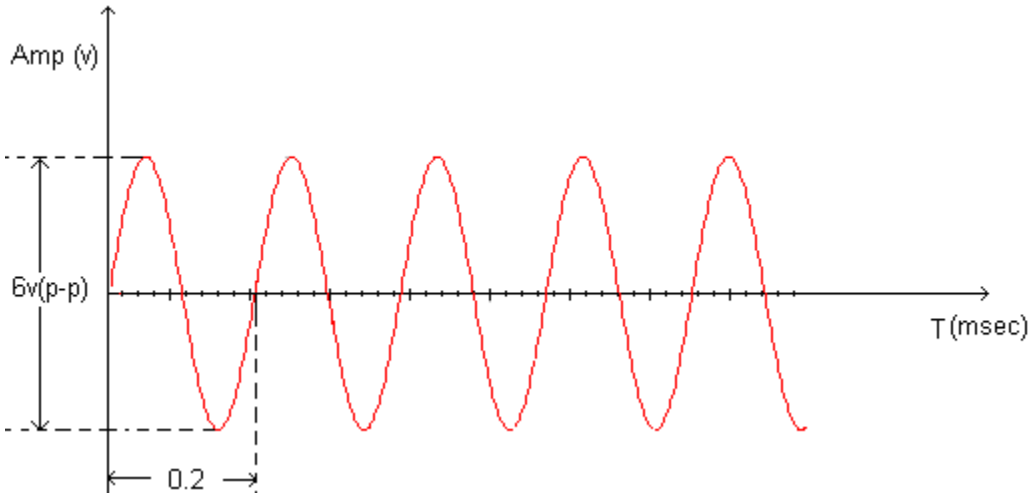

Fig B: Frequency of oscillations

Precautions:

1. Connections must be done very carefully.
2. Readings should be taken without parallax error.

Result:

The frequency of Hartley oscillator is practically observed.

5(b). COLPITTS OSCILLATOR

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Aim:

To measure the frequency of the Colpitts Oscillator

Apparatus Required:

S. No	Name of the Component/Equipment	Specifications	Quantity
1.	Colpitts Oscillator Circuit Board	___	1
2.	Cathode Ray Oscilloscope	20 MHz	1

Theory:

In the Colpitts oscillator shown in fig 1, Z_1, and Z_2 are capacitors and Z_3 is an inductor. The resistors R and R_2 and R_E provide the necessary DC bias to the transistor. C_E is a bypass capacitor C_{C1} and C_{C2} are coupling capacitors. The feedback network consisting of capacitors C_1 and C_2, inductor L determine the frequency of the oscillator.

When the supply voltage $+V_{cc}$ is switched ON, a transient current is produced in the tank circuit, and consequently damped harmonic oscillations are setup in the circuit. The current in tank circuit produces AC voltages across C_1 and C_2. As terminal 3 is earthed, it will be at zero potential.

If terminal is at positive potential with respect to 3 at any instant, then terminal 2 will be at negative potential with respect to 3 at the same instant. Thus the phase difference between the terminals 1 and 2 is always 180^0. In the CE mode, the transistor provides the phase difference of 180^0 between the input and output. Therefore the total phase shift is 360^0. The frequency of oscillations is

$$f = 1/2\pi\sqrt{LC} \quad \text{where } 1/C = 1/C_1 + 1/C_2.$$

Circuit Diagram:

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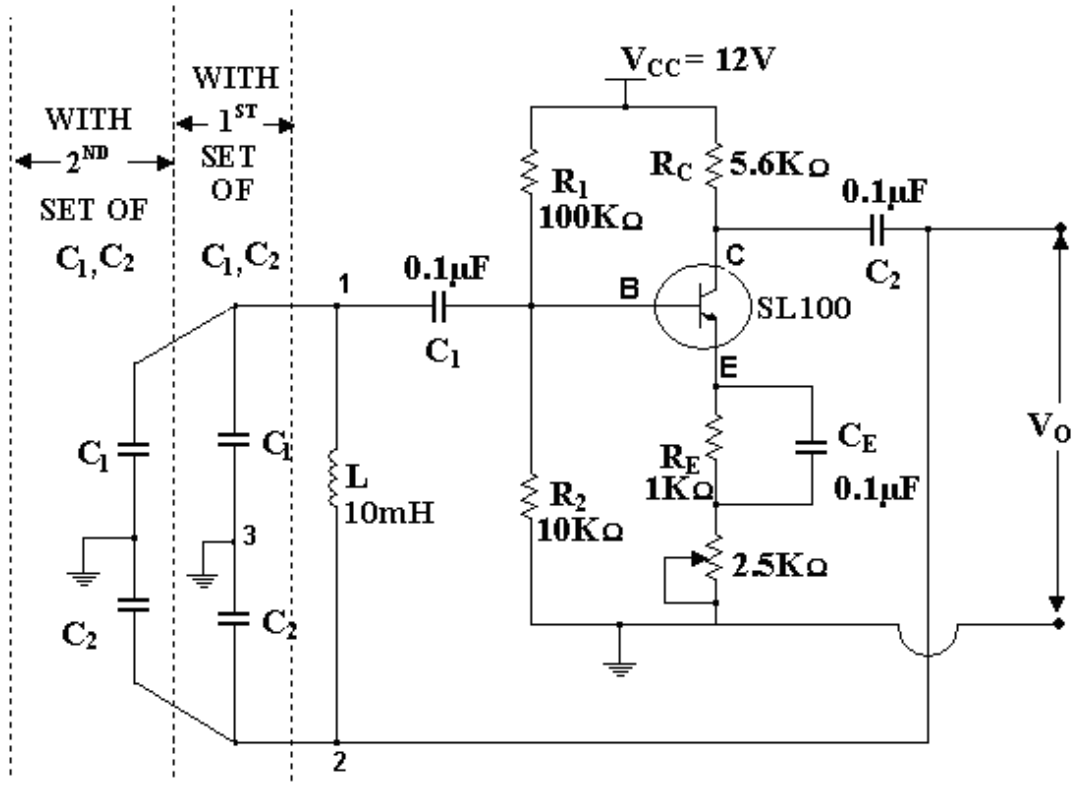

Fig A: Colpitts Oscillator

Procedure:

1. Switch on the power supply by inserting the power card in AC mains
2. Connect one pair of capacitors as C_1 and C_2 as shown in the dotted lines of Fig A.
3. Observe the output of the oscillator on a CRO. Adjust the potentiometer R_E on the front panel until we get an undistorted output. Note down the repetition period (T) of observed signal. Compute f_O= 1/T (R_E can adjust the gain of amplifier).
4. Calculate the theoretical frequency of the circuit using formulae.
5. Repeat the step 2 and 4 for the second pair of capacitors C_1 and C_2. Tabulate the results as below.

Tabular Form:

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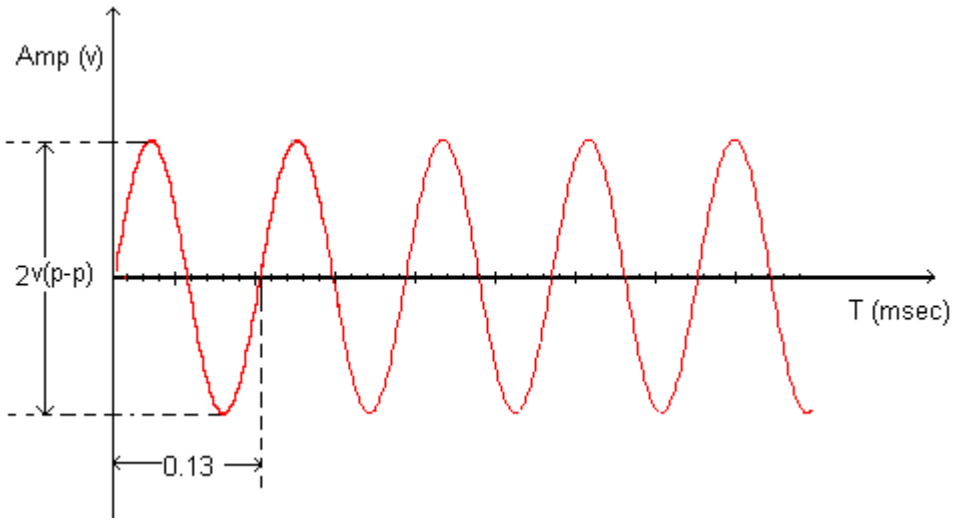
S.No	Condition	Theoretical Frequency (KHz)	Practical frequency(KHz)	%Error
1	$C_1=C_2=0.01\mu F$	22.507		
2	$C_1=C_2=0.1\mu F$	7.117		

Model Graph:



Precautions:

1. Connections must be done very carefully.

2. Readings should be taken without parallax error.

Result:

The frequency of Colpitts Oscillators is practically determined.

6. CLASS B COMPLEMENTARY SYMMETRY

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POWER AMPLIFIER

Aim:

1. Design a complementary symmetry power amplifier to deliver maximum power to 10 Ohm load resistor.
2. Simulate the design circuit.
3. Develop the hard ware for design circuit.
4 Compare simulation results with practical results.

Apparatus:

Sl.No	Name of the Component /equipment	Specifications	Qty
1	Power transistor (BD139)	V_{CE} =60V V_{BE} = 100V IC = 100mA hfe = 40 -160	1
2	Resistor (designed values)	Power rating=0.5W Carbon type	4
3	Capacitors(designed values)	Electrolytic type Voltage rating= 1.6v	3
4	Inductor(designed values)	Operating temp =ambient	1
5	Function Generator	0 -1MHZ	1
6	Cathode Ray Oscilloscope	20MHZ	1
7	Regulated Power Supply	0-30V,1Amp	1

Theory: In complementary symmetry class B power amplifier one is p-n-p and other transistor is n-p-n. In the positive half cycle of input signal the transistor Q_1 gets driven into active region

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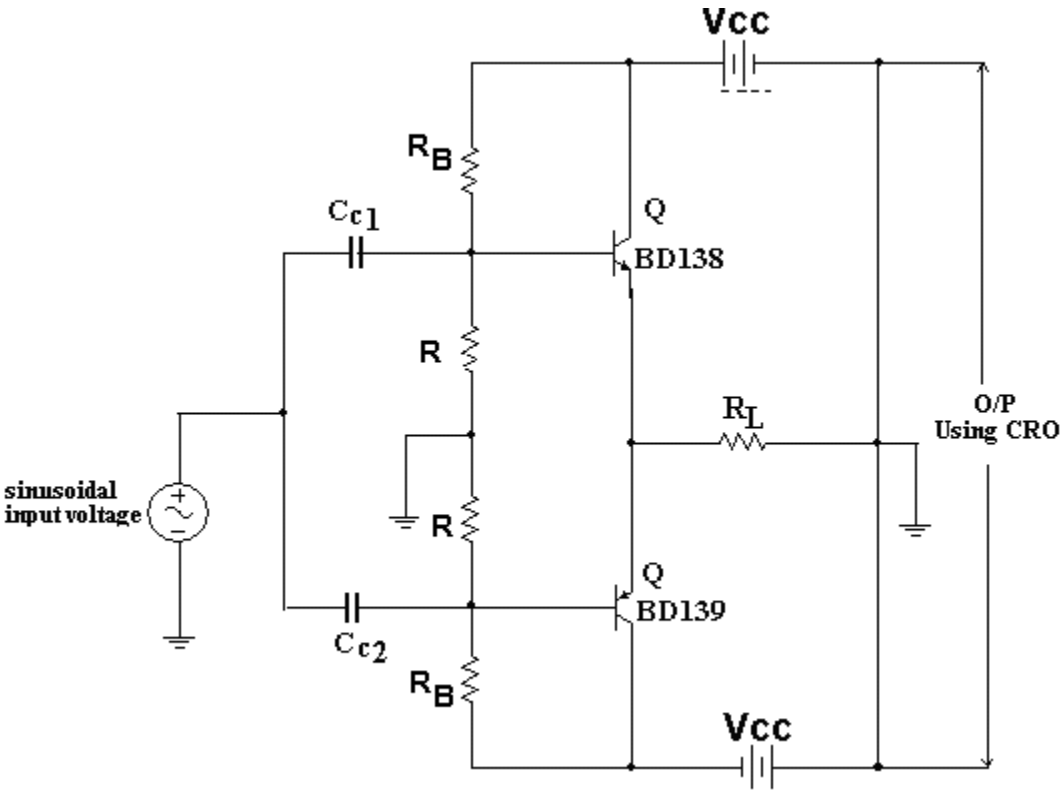
and starts conducting. The same signal gets applied to the base of the Q_2. it ,remains in off condition, during the positive half cycle. During the negative half cycle of the signal the transistor Q_2 p-n-p gets biased into conduction. While Q_1 gets driven into cut off region. Hence only Q_2 conducts during negative half cycle of the input, producing negative half cycle across the load.

Circuit Diagram:



Design Equations:

Given data: $P_{L\,(MAX)}$ =5 W, R_L= 10Ω, f = 1KHZ

1. Selection of V_{CC}:-

$$P_{L\,(MAX)} = V_{CC}^{\,2} / 2R_L$$

$$V_{CC}^{\,2} = P_{L\,(MAX)}\, 2R_L$$

$$= 100V$$

$$V_{CC} = 10V$$

Selection R and R_B:-

$$V_{BB} = V_{BE} = 0.6V \text{ , assume } R = 150\Omega$$

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$V_{BB}=V_{CC}.R / (R+R_B)$

$0.6 = 10*150/ (150+R_B)$

$R_B = 2.35K\Omega$

Capacitor calculations:-

To provide low reactances almost short circuit at the operating frequency

f=1KHZ.

$X_{CC1} = XC_{C2} = (R \backslash\backslash R_B) / 10$

$= (150)(2350)/(10)(2550) = 14.1$

$C_{C1} = C_{C2} = 1/ 2 \pi f X_{CC1} = 11.28\mu F$

Procedure:

1. Connect the circuit diagram and supply the required DC supply.
2. Apply the AC signal at the input and keep the frequency at 1 KHz and connect the power o/p meter at the output. Change the Load resistance in steps for each value of impedance and note down the output power.
3. Plot the graph between o/p power and load impedance. From this graph find the impedance for which the output power is maximum. This is the value of optimum load.
4. Select load impedance which is equal to 0V or near about the optimum load. See the wave form of the o/p of the C.R.O.
5. Calculate the power sensitivity at a maximum power o/p using the relation.

Tabular Form:

Input power = 360mW

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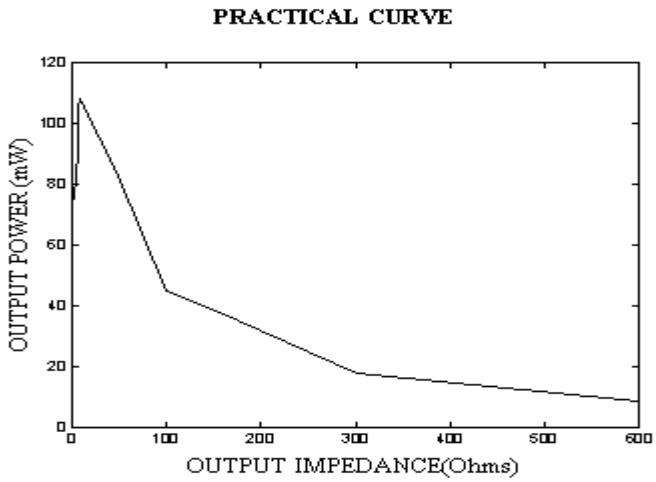
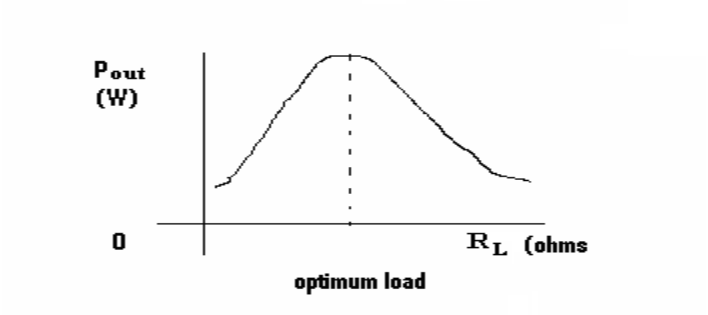
S.No	Output Impedance(Ω)	Input power (p_i) (mW)	OutputPower(p_o)(mW)	N=(Po)/(Pi) x100



Model Graph:



Precautions:

1. Connections should be made care fully.
2. Take the readings with out parallax error.
3. Avoid loose connections.

Result: Class B complementary symmetry amplifier is designed for given specifications and its performance is observed.

7.DSB-SC Modulation and Demodulation

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Aim:

To generate AM-Double Side Band Suppressed Carrier (DSB-SC) signal.

Apparatus Required:

Name of the Component/Equipment	Specifications/Range	Quantity
IC 1496	Wide frequency response up to 100 MHz Internal power dissipation – 500mw(MAX)	1
Resistors	6.8KΩ 10 KΩ, 3.9 KΩ 1KΩ ,51 KΩ	1 2 each 3 each
Capacitors	0.1 μF	4
Variable Resistor (Linear Pot)	0-50KΩ	1
CRO	100MHz	1
Function Generator	1MHz	2
Regulated Power Supply	0-30 v, 1A	1

Theory:

Balanced modulator is used for generating DSB-SC signal. A balanced modulator consists of two standard amplitude modulators arranged in a balanced configuration so as to suppress the carrier wave. The two modulators are identical except the reversal of sign of the modulating signal applied to them.

Circuit Diagram:

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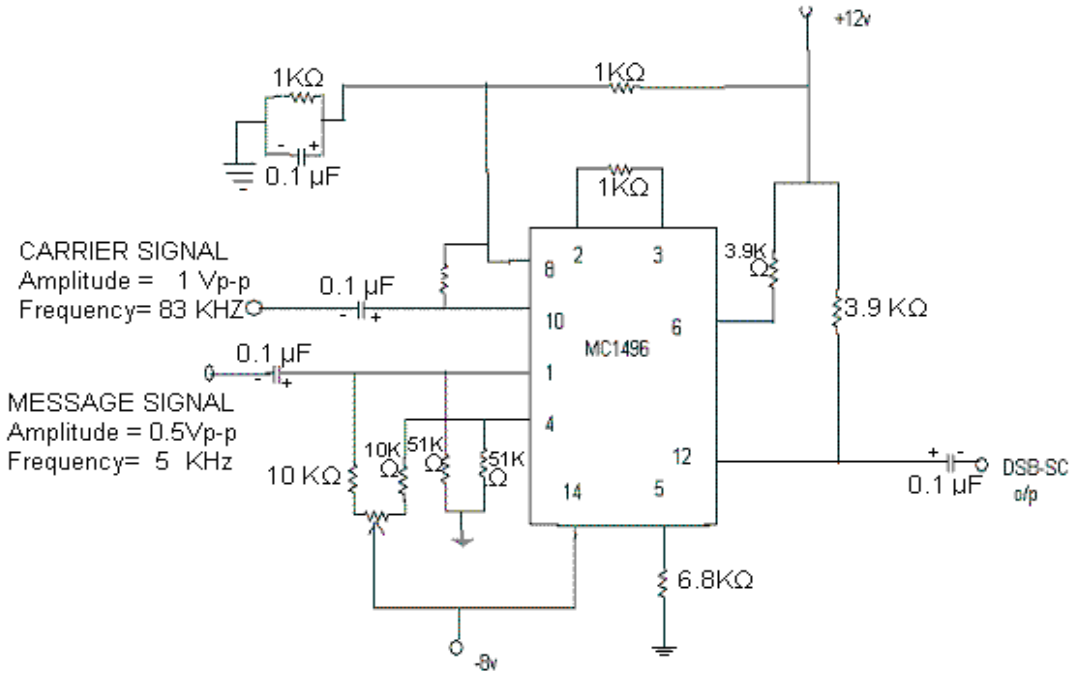

Fig.1. Balanced Modulator Circuit

Procedure:

1. Connect the circuit diagram as shown in Fig.1.
2. An Carrier signal of 1Vp-p amplitude and frequency of 83 KHz is applied as carrier to pin no.10.
3. An AF signal of 0.5Vp-p amplitude and frequency of 5 KHz is given as message signal to pin no.1.
4. Observe the DSB-SC waveform at pin no.12.

Sample readings:

Signal	AMPLITUDE (Volts)	Frequency (Hz)
Message signal	0.5V	5 KHz
Carrier signal	1V	83.3KHz
DSB-SC Signal	1.92V p-p	---------

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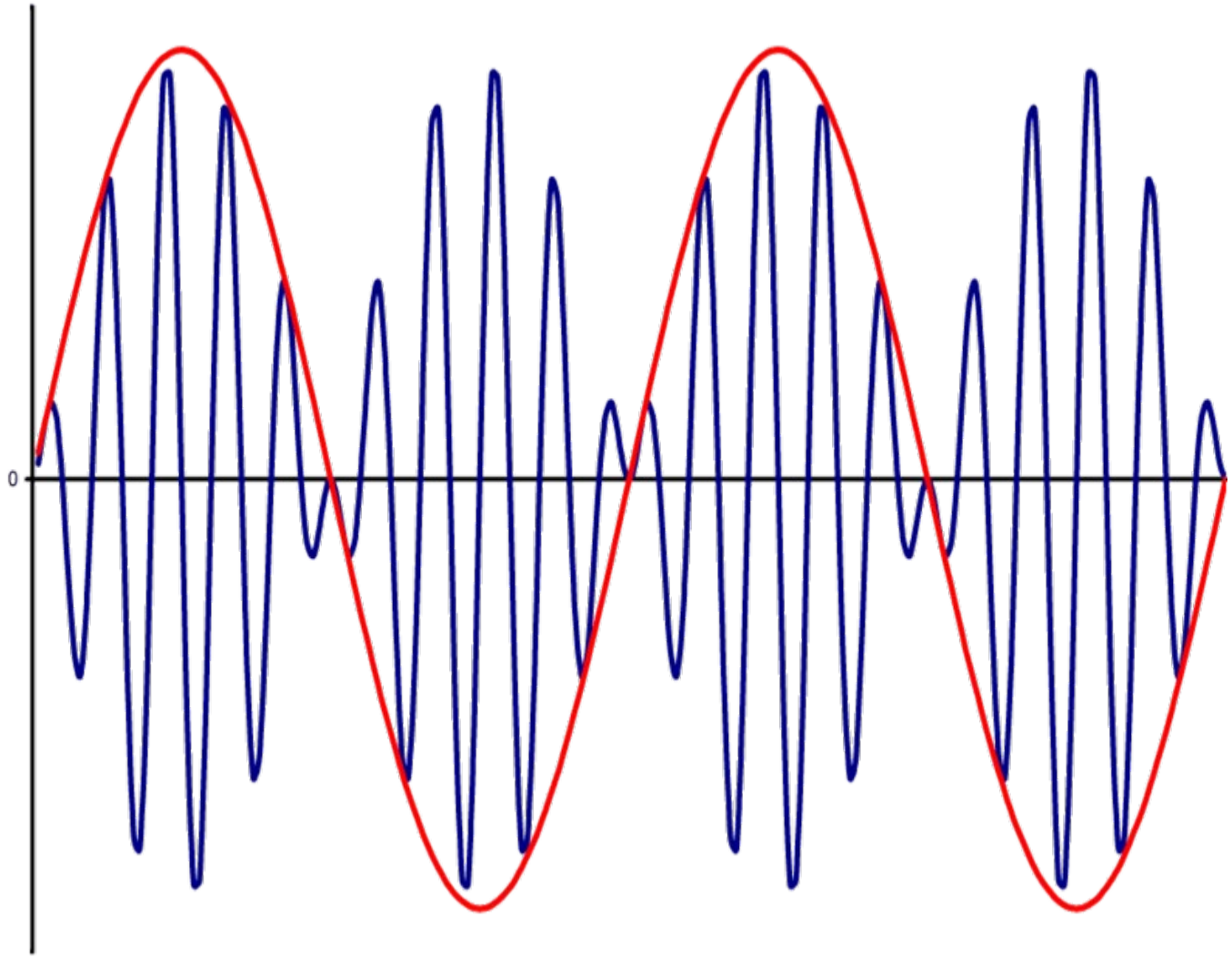
Waveforms:



Precautions:

1. Check the connections before giving the supply
2. Observations should be done carefully

Observe:

Phase reversal in DSB-SC Signal is occur at the zero crossing of modulating signal.

8.SSB Modulation and Demodulatiom

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Aim: To generate the SSB modulated wave.

Apparatus Required:

Name of the Component/Equipment	Specifications	Quantity
SSB system trainer board	---	1
CRO	30MHz	1

Theory:

An SSB signal is produced by passing the DSB signal through a highly selective band pass filter. This filter selects either the upper or the lower sideband. Hence transmission bandwidth can be cut by half if one sideband is entirely suppressed. This leads to single-sideband modulation (SSB). In SSB modulation bandwidth saving is accompanied by a considerable increase in equipment complexity.

Circuit Diagram:

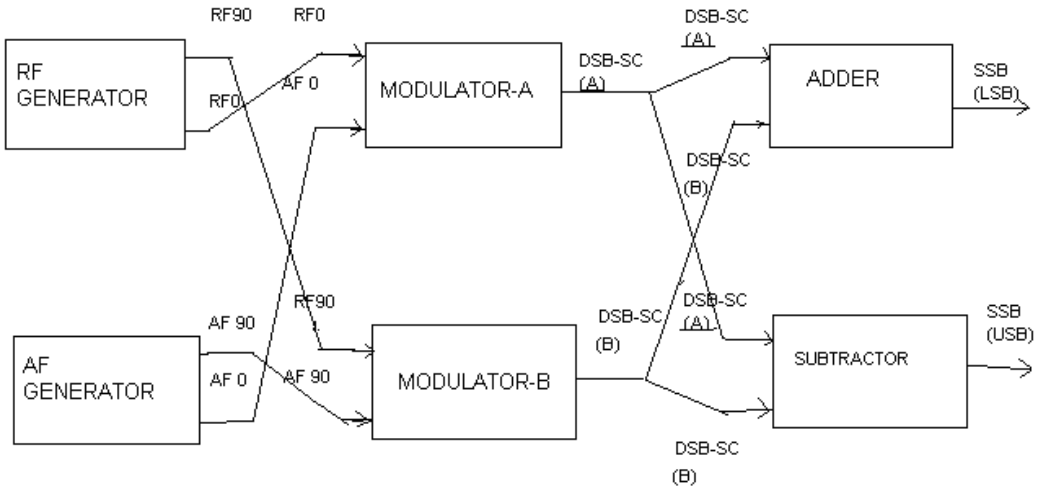

Fig. 1 Single Side Band system

Procedure:

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1. Switch on the trainer and measure the output of the regulated power supply i.e., ±12V and -8V.
2. Observe the output of the RF generator using CRO. There are 2 outputs from the RF generator, one is direct output and another is 90° out of phase with the direct output. The output frequency is 100 KHz and the amplitude is ≥ $0.2V_{PP}$. (Potentiometers are provided to vary the output amplitude).
3. Observe the output of the AF generator, using CRO. There are 2 outputs from the AF generator, one is direct output and another is 90° out of phase with the direct output. A switch is provided to select the required frequency (2 KHz, 4KHz or 6 KHz). AGC potentiometer is provided to adjust the gain of the oscillator (or to set the output to good shape). The oscillator output has amplitude ≅ $10V_{PP}$. This amplitude can be varied using the potentiometers provided.
4. Measure and record the RF signal frequency using frequency counter. (or CRO).
5. Set the amplitudes of the RF signals to 0.1 V_{p-p} and connect direct signal to one balanced modulator and 90° phase shift signal to another balanced modulator.
6. Select the required frequency (2KHz, 4KHz or 6KHz) of the AF generator with the help of switch and adjust the AGC potentiometer until the output amplitude is ≅ 10 V_{PP} (when amplitude controls are in maximum condition).
7. Measure and record the AF signal frequency using frequency counter (or CRO).
8. Set the AF signal amplitudes to 8 V_{p-p} using amplitude control and connect to the balanced modulators.
9. Observe the outputs of both the balanced modulators simultaneously using Dual trace oscilloscope and adjust the balance control until desired output wave forms (DSB-SC).
10. To get SSB lower side band signal, connect balanced modulator output (DSB_SC) signals to subtract or.
11. Measure and record the SSB signal frequency.
12. Calculate theoretical frequency of SSB (LSB) and compare it with the practical value.
    LSB frequency = RF frequency – AF frequency
13. To get SSB upper side band signal, connect the output of the balanced modulator to the summer circuit.
14. Measure and record the SSB upper side band signal frequency.
15. Calculate theoretical value of the SSB(USB) frequency and compare it with practical value.
    USB frequency = RF frequency + AF frequency

Sample readings:

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Signal	Amplitude (volts)	Frequency (KHz)
Message signal	2	1
Carrier signal	2	100
SSB (LSB)	0.5	98.54
SSB (USB)	0.42	101.4

Waveforms:

Precautions:

1. Check the connections before giving the power supply
2. Observations should be done careful

9. Frequency Modulation And Demodulation

Aim: 1. To generate frequency modulated signal and determine the modulation index and bandwidth for various values of amplitude and frequency of modulating signal.

2. To demodulate a Frequency Modulated signal using FM detector.

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Apparatus required:

Name of the Component/Equipment	Specifications/Range	Quantity
IC 566	Operating voltage –Max-24 Volts Operating current-Max.12.5 mA	1
IC 8038	Power dissipation – 750mW Supply voltage - ±18V or 36V total	1
IC 565	Power dissipation -1400mw Supply voltage - ±12V	1
Resistors	15 K Ω, 10 K Ω, 1.8 K Ω, 39 K Ω, 560 Ω	1,2,1 2,2
Capacitors	470 pF, 0.1μF 100pF , 0.001μF	2,1 1,1 each
CRO	100MHz	1
Function Generator	1MHz	2
Regulated Power Supply	0-30 v, 1A	1

Theory: The process, in which the frequency of the carrier is varied in accordance with the instantaneous amplitude of the modulating signal, is called “Frequency Modulation”. The FM signal is expressed as

$$s(t) = A_c \cos\left(2\pi f_c + \beta \sin\left(2\pi f_m t\right)\right)$$

Where A_C is amplitude of the carrier signal, f_C is the carrier frequency

β is the modulation index of the FM wave

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Circuit Diagrams:

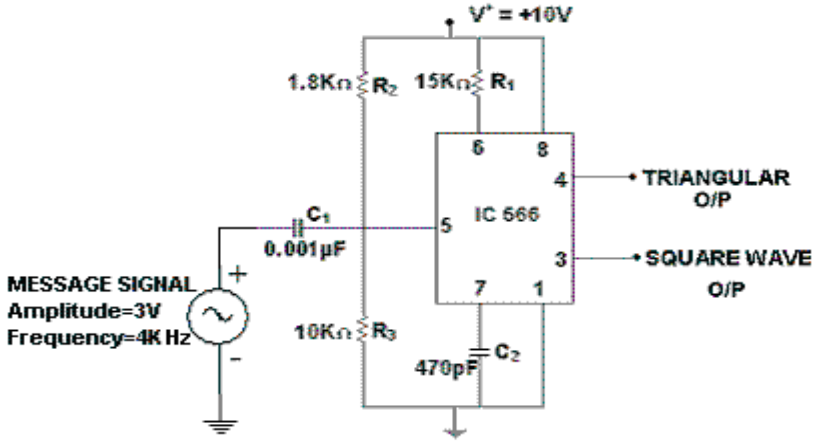

Fig.1. FM Modulator Using IC 566

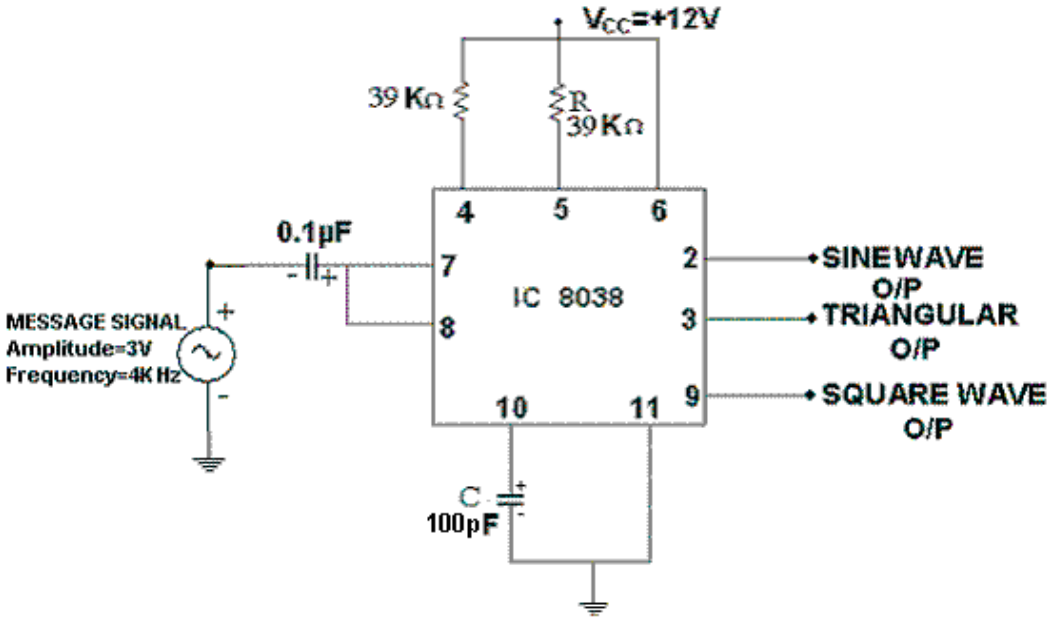

Fig.2. FM Modulator Circuit

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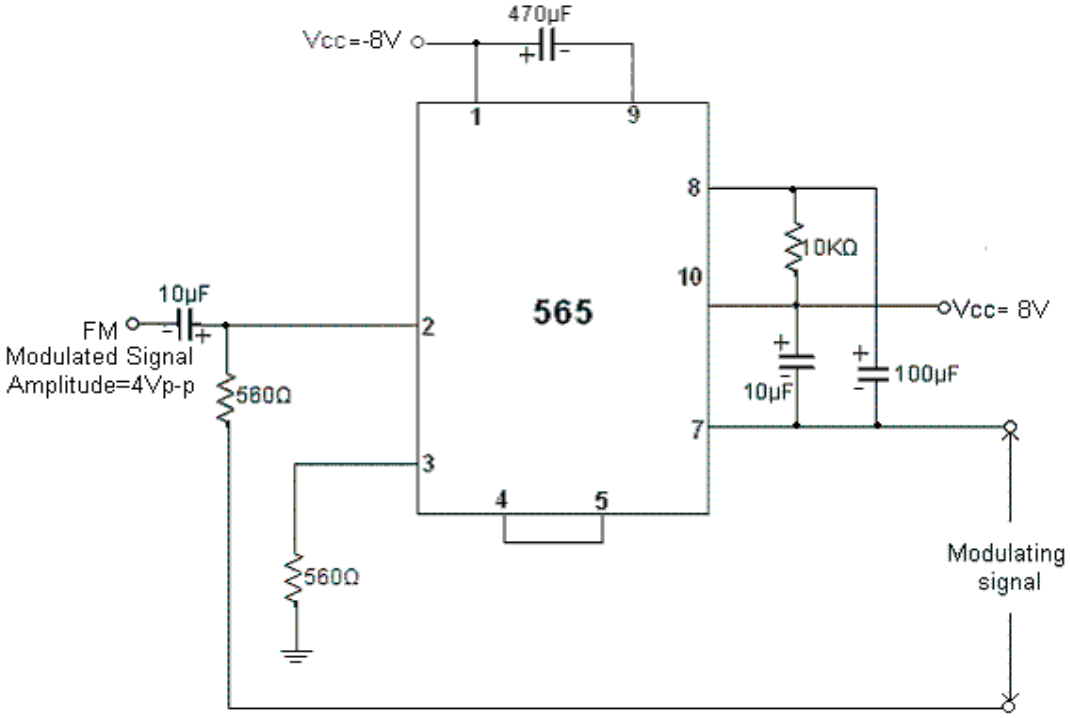

Fig.3. FM Demodulator Circuit

Procedure:

Modulation:

1. The circuit is connected as per the circuit diagram shown in Fig.2(Fig.1 for IC 566)
2. Without giving modulating signal observe the carrier signal at pin no.2 (at pin no.3 for IC 566). Measure amplitude and frequency of the carrier signal. To obtain carrier signal of desired frequency, find value of R from f = 1/ (2ΠRC) taking C=100pF.
3. Apply the sinusoidal modulating signal of frequency 4KHz and amplitude 3Vp-p at pin no.7. (pin no.5 for IC 566)

   Now slowly increase the amplitude of modulating signal and measure f_{min} and maximum frequency deviation Δf at each step. Evaluate the modulating index ($m_f = \beta$) using $\Delta f / f_m$ where $\Delta f = |f_c - f_{min}|$. Calculate Band width. BW = $2(\beta + 1)f_m = 2(\Delta f + f_m)$
4. Repeat step 4 by varying frequency of the modulating signal.

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Demodulation:

1. Connections are made as per circuit diagram shown in Fig.3
2. Check the functioning of PLL (IC 565) by giving square wave to input and observing the output
3. Frequency of input signal is varied till input and output are locked.
4. Now modulated signal is fed as input and observe the demodulated signal (output) on CRO.
5. Draw the demodulated wave form.

Sample readings:

Table: 1 f_c = 45KHz

S.No.	f_m(KHz)	T_{max} (µsec)	f_{min}(KHz)	Δf(KHz)	β	BW (KHz)

Table 2: f_m = 4 KHz, f_c = 45 KHz

S.No.	A_m (Volts)	$T_{(\mu sec)}$	f_{min}(KHz)	Δf (KHz)	β	BW(KHZ)

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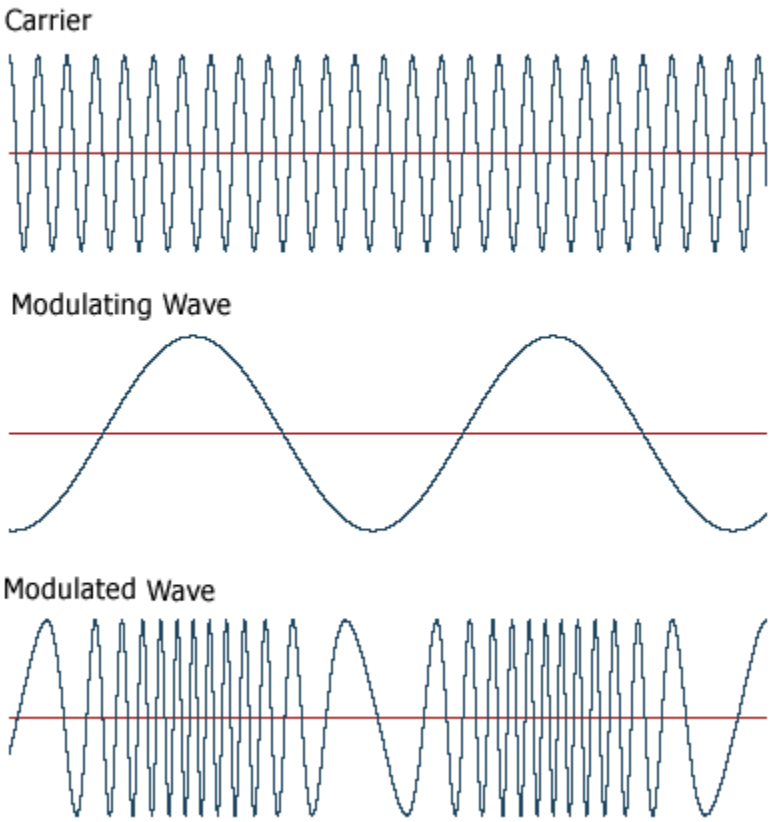
Waveforms:



Precautions:

1. Check the connections before giving the power supply
2. observations should be done carefully

10. Pre-Emphasis & De-Emphasis

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Aim:

I) To observe the effects of pre-emphasis on given input signal.

ii) To observe the effects of De-emphasis on given input signal.

Apparatus Required:

Name of the Component/Equipment	Specifications/Range	Quantity
Transistor (BC 107)	f_T = 300 MHz P_d = 1W I_c(max) = 100 mA	1
Resistors	10 KΩ, 7.5 KΩ, 6.8 KΩ	1 each
Capacitors	10 nF 0.1 μF	1 2
CRO	20MHZ	1
Function Generator	1MHZ	1
Regulated Power Supply	0-30V, 1A	1

Theory:

The noise has a effect on the higher modulating frequencies than on the lower ones. Thus, if the higher frequencies were artificially boosted at the transmitter and correspondingly cut at the receiver, an improvement in noise immunity could be expected, there by increasing the SNR ratio. This boosting of the higher modulating frequencies at the transmitter is known as pre-emphasis and the compensation at the receiver is called de-emphasis.

Circuit Diagrams:

For Pre-emphasis:

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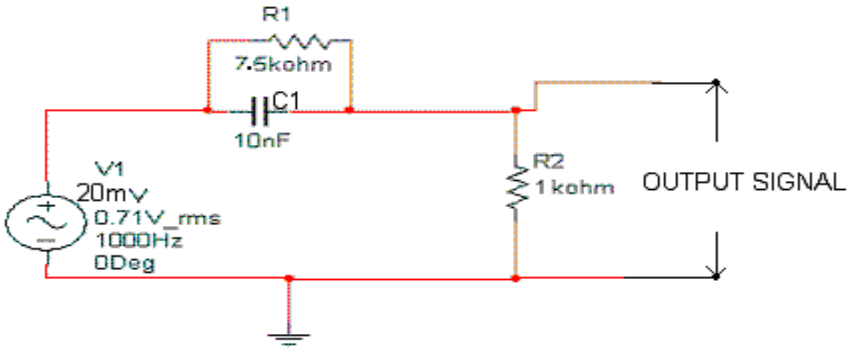

Fig.1. Pre-emphasis circuit

For De-emphasis:

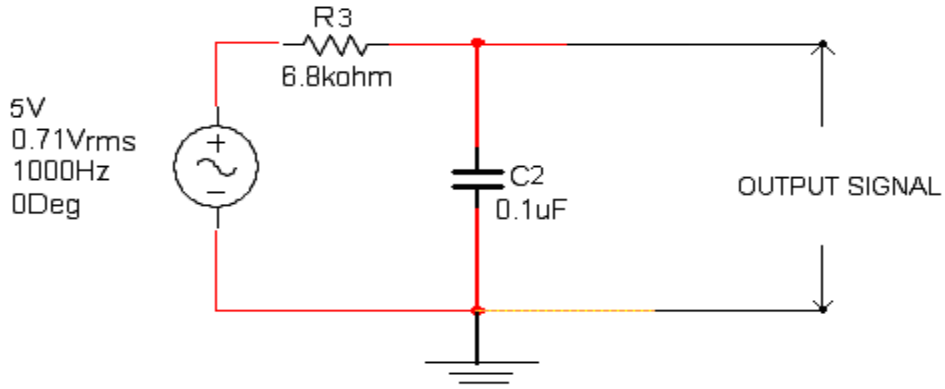

Fig.2. De-emphasis circuit

Procedure:

1. Connect the circuit as per circuit diagram as shown in Fig.1.
2. Apply the sinusoidal signal of amplitude 20mV as input signal to pre emphasis circuit.
3. Then by increasing the input signal frequency from 500Hz to 20KHz, observe the output voltage (v_o) and calculate gain (20 log (v_o/v_i).
4. Plot the graph between gain Vs frequency.
5. Repeat above steps 2 to 4 for de-emphasis circuit (shown in Fig.2). by applying the sinusoidal signal of 5V as input signal

Sample readings:

Table1: Pre-emphasis V_i = 20mV

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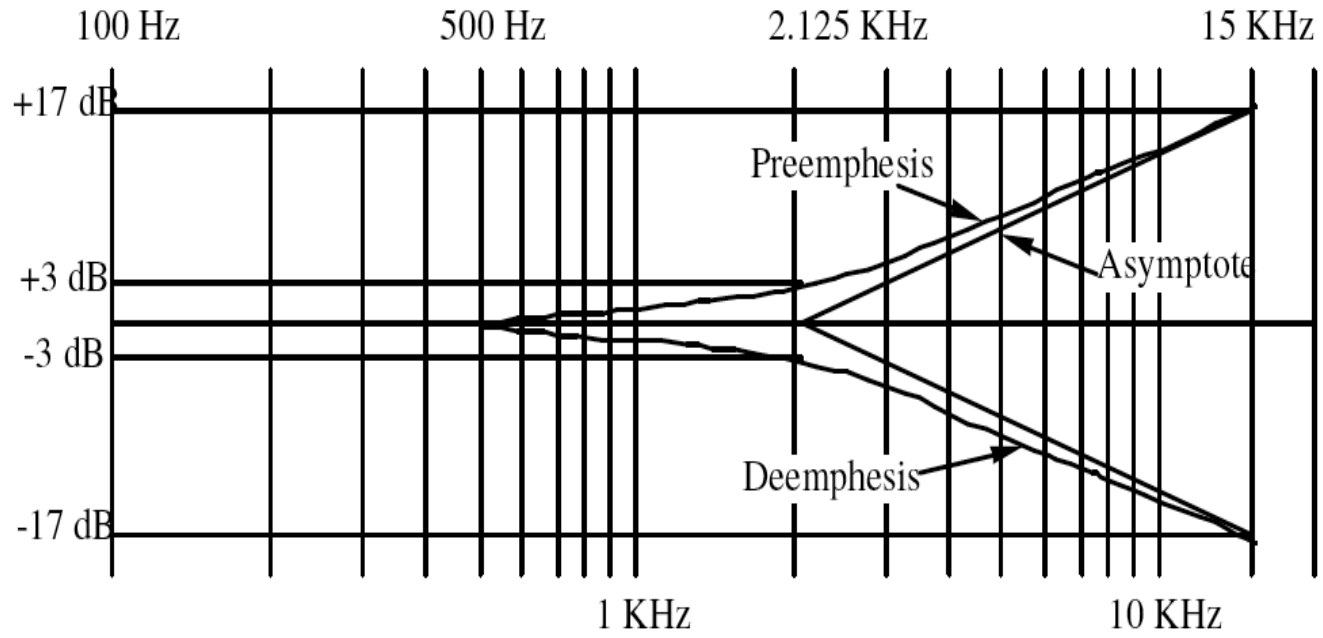
Frequency(KHz)	Vo(mV)	Gain in dB(20 log V_o/V_i)

Table2: De-emphasis V_i = 5v

Frequency(KHz)	Vo(Volts)	Gain in dB(20 log V_o/V_i)

Graphs:



Precautions:

1. Check the connections before giving the power supply

Observation should be done carefully

11. SAMPLING THEOREM VERIFICATION

Aim: To verify the sampling theorem.

Apparatus Required:

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1. Sampling theorem verification trainer kit

2. Function Generator (1MHz)

3. Dual trace oscilloscope (20 MHz)

Theory:

The analog signal can be converted to a discrete time signal by a process called sampling. The sampling theorem for a band limited signal of finite energy can be stated as,

''A band limited signal of finite energy, which has no frequency component higher than W Hz is completely described by specifying the values of the signal at instants of time separated by 1/2W seconds.''

It can be recovered from knowledge of samples taken at the rate of 2W per second.

Circuit Diagram:

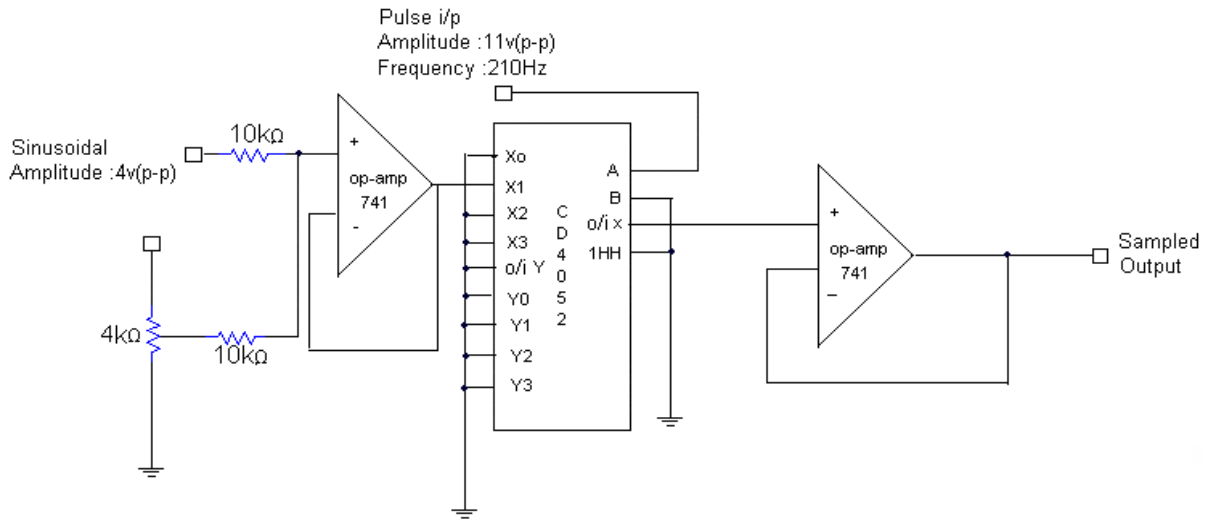

Fig: 1 Sampling Circuit

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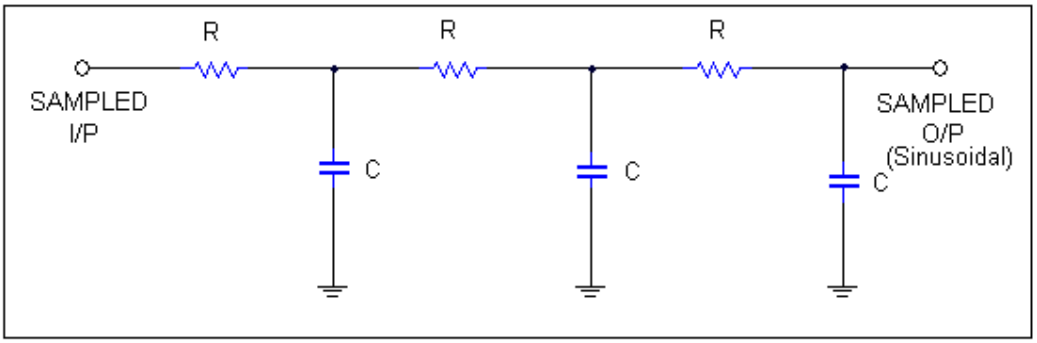

Fig: 2 Reconstructing Circuit

Procedure:

1. The circuit is connected as per the circuit diagram shown in the fig 1.
2. Switch on the power supply. And set at +11V and -11V.
3. Apply the sinusoidal signal of approximately 4V (p-p) at 105Hz frequency and pulse signal of 11V (p-p) with frequency between 100Hz and 4 KHz.
4. Connect the sampling circuit output and AF signal to the two inputs of oscilloscope
5. Initially set the potentiometer to minimum level and sampling frequency to 200Hz and observe the output on the CRO. Now by adjusting the potentiometer, vary the amplitude of modulating signal and observe the output of sampling circuit. Note that the amplitude of the sampling pulses will be varying in accordance with the amplitude of the modulating signal.
6. Design the reconstructing circuit. Depending on sampling frequency, R & C values are calculated using the relations $F_s = 1/T_s$, $T_s = RC$. Choosing an appropriate value for C, R can be found using the relation $R=T_s/C$
7. Connect the sampling circuit output to the reconstructing circuit shown in Fig 2
8. Observe the output of the reconstructing circuit (AF signal) for different sampling frequencies. The original AF signal would appear only when the sampling frequency is 200Hz or more.

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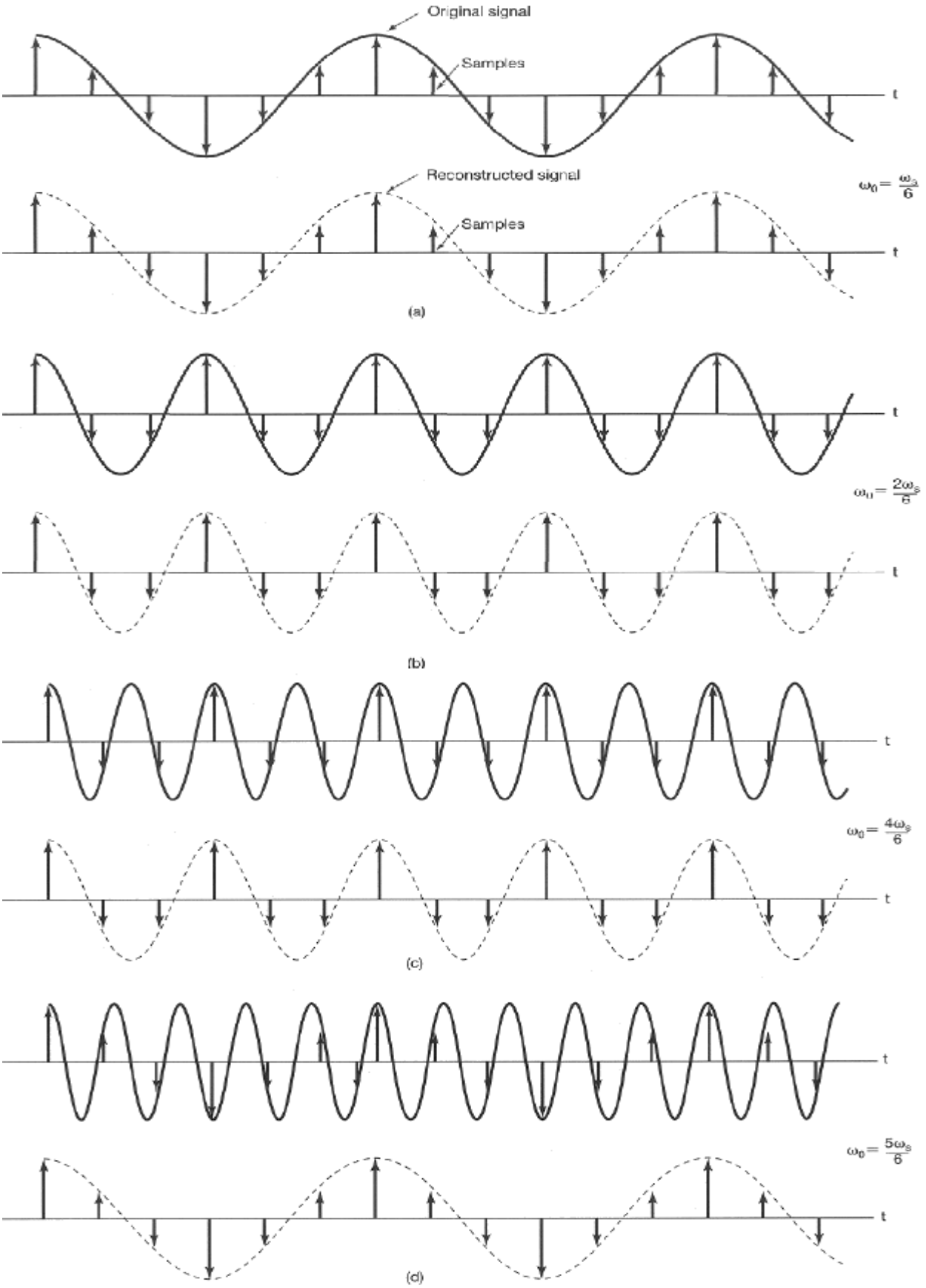

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12. PULSE AMPLITUDE MODULATION & DEMODULATION

Aim: To generate the Pulse Amplitude modulated and demodulated signals.

Apparatus required:

Name of the Apparatus	Specifications/Range	Quantity
Resistors	1KΩ, 10KΩ, 100KΩ, 5.8KΩ, 2.2KΩ,	Each one
Transistor	BC 107	2
Capacitor	10μF, 0.001μF	each one
CRO	30MHz	1
Function generator	1MHz	1
Regulated Power Supply	0-30V,1A	1
CRO Probes	---	1

Theory:

PAM is the simplest form of data modulation .The amplitude of uniformly spaced pulses is varied in proportion to the corresponding sample values of a continuous message m (t).

A PAM waveform consists of a sequence of flat-topped pulses. The amplitude of each pulse corresponds to the value of the message signal x (t) at the leading edge of the pulse.

The pulse amplitude modulation is the process in which the amplitudes of regularity spaced rectangular pulses vary with the instantaneous sample values of a continuous message signal in a one-one fashion. A PAM wave is represented mathematically as,

$$S(t) = \sum_{N=-\infty}^{\infty} [1+K_a x (nT_s)] P (t-nT_s)$$

Where

$x (nT_s)$ ==> represents the n^{th} sample of the message signal x(t)

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K= ==> is the sampling period.

K_a ==> a constant called amplitude sensitivity

P (t) ==>denotes a pulse

PAM is of two types

1) Double polarity PAM ==> This is the PAM wave which consists of both positive and negative pulses shown as

2) Single polarity PAM ==> This consists of PAM wave of only either negative (or)

Positive pulses. In this the fixed dc level is added to the signal to ensure single polarity signal. It is represented as

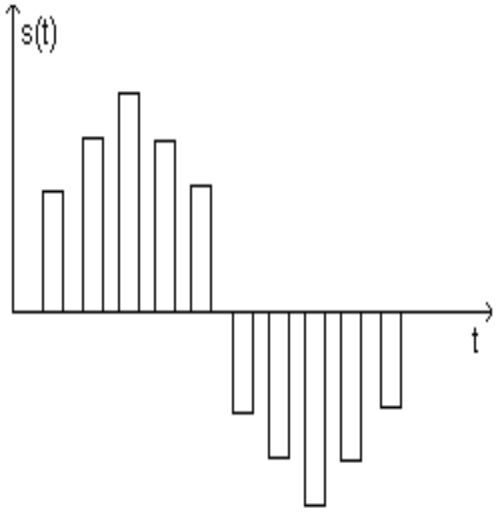

Fig: 1 Bipolar PAM signal

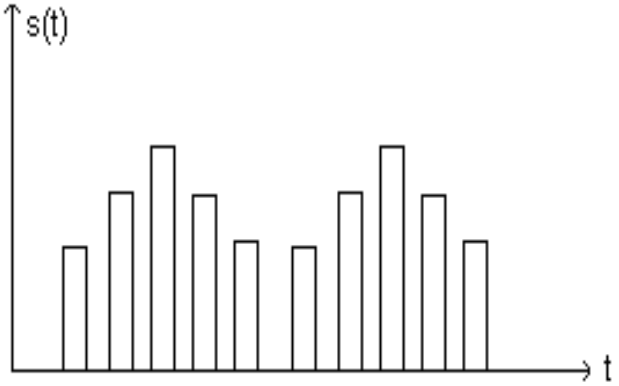

Fig: 2 Single polarity PAM

Circuit Diagram:

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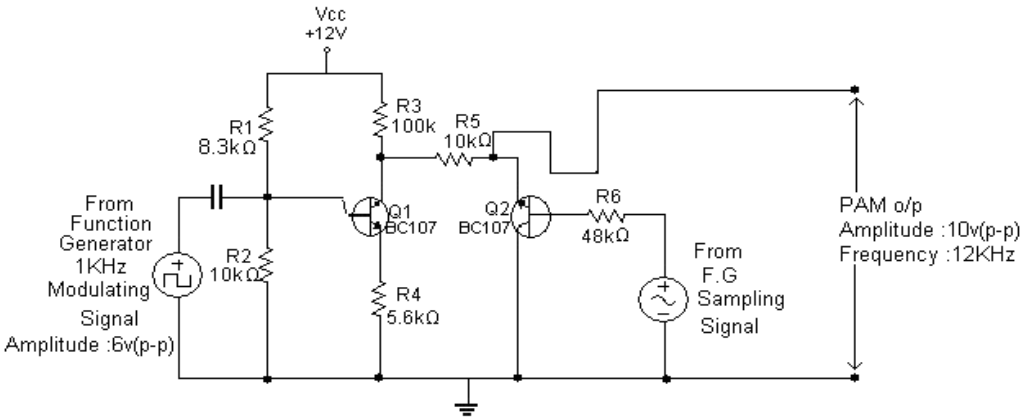

Fig: 3 Pulse Amplitude Modulation Circuit

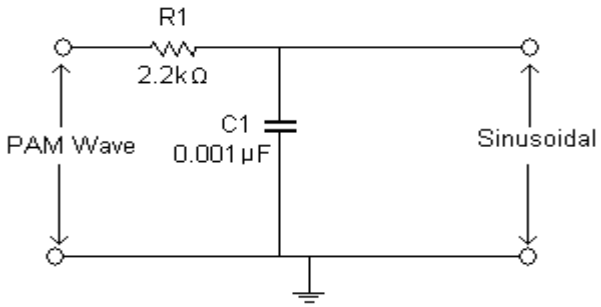

Fig: 4 Demodulation Circuit

Procedure:

1. Connect the circuit as per the circuit diagram shown in the fig 3
2. Set the modulating frequency to 1KHz and sampling frequency to 12KHz
3. Observe the o/p on CRO i.e. PAM wave.
4. Measure the levels of E_{max} & E_{min}.
5. Feed the modulated wave to the low pass filter as in fig 4.
6. The output observed on CRO will be the demodulated wave.
7. Note down the amplitude (p-p) and time period of the demodulated wave. Vary the amplitude and frequency of modulating signal. Observe and note down the changes in output.
8. Plot the wave forms on graph sheet.

13(a). PULSE WIDTH MODULATION AND DEMODULATION

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Aim: To generate the pulse width modulated and demodulated signals

Apparatus required:

Name of the Apparatus	Specifications/Range	Quantity
Resistors	1.2kΩ, 1.5 kΩ, 8.2 kΩ	1,1,2
Capacitors	0.01 μF, 1 μF	2,2
Diode	0A79	1
CRO	0-30, MHz	1
Function Generator	1MHz	1
RPS	0-30v,1A	1
IC 555	Operating tem :SE 555 -55°C to 125°C NE 555 0° to 70°C Supply voltage :+5V to +18V Timing :μSec to Hours Sink current :200mA Temperature stability :50 PPM/°C change in temp or 0-005% /°C.	1
CRO Probes	--	1

Theory:

Pulse Time Modulation is also known as Pulse Width Modulation or Pulse Length Modulation. In PWM, the samples of the message signal are used to vary the duration of the individual pulses. Width may be varied by varying the time of occurrence of leading edge, the trailing edge or both edges of the pulse in accordance with modulating wave. It is also called Pulse Duration Modulation.

Circuit Diagram:

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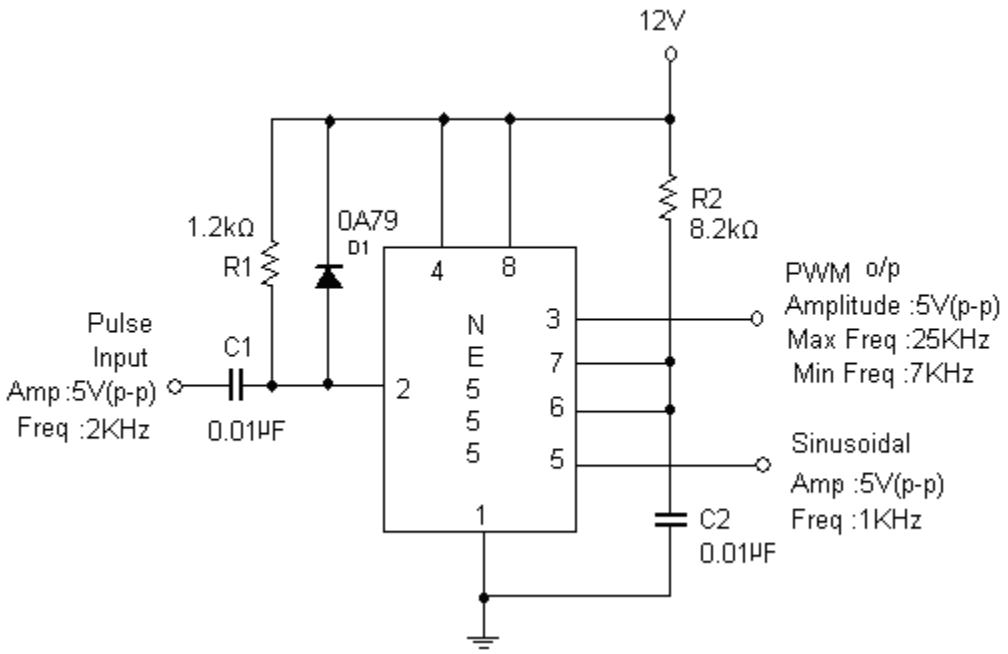

Fig: 1 Pulse Width Modulation Circuit

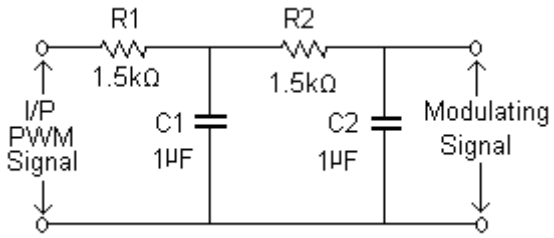

Fig: 2 Demodulation Circuit

Procedure:

1. Connect the circuit as per circuit diagram shown in fig 1.
2. Apply a trigger signal (Pulse wave) of frequency 2 KHz with amplitude of 5v (p-p).
3. Observe the sample signal at the pin3.
4. Apply the ac signal at the pin 5 and vary the amplitude.
5. Note that as the control voltage is varied output pulse width is also varied.

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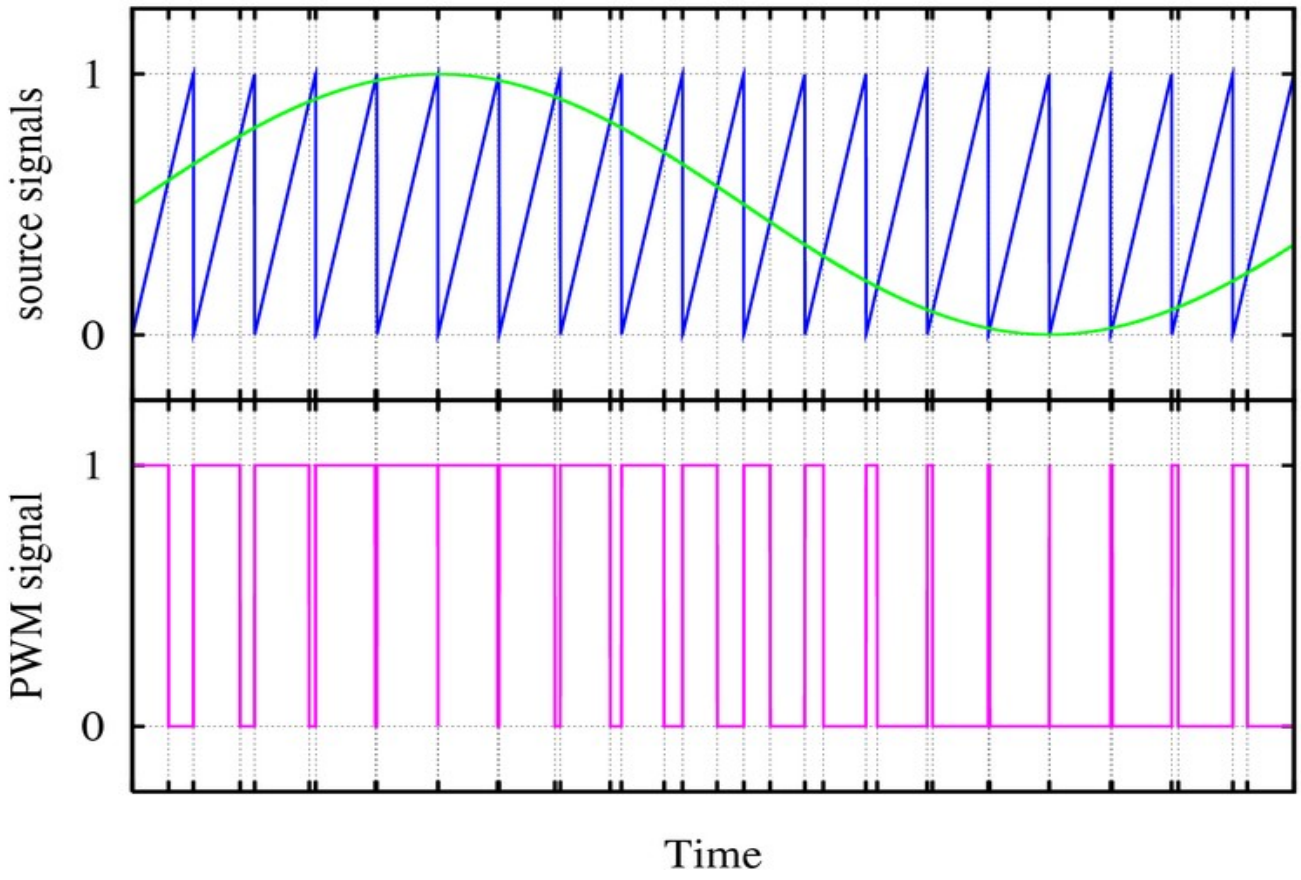
6. Observe that the pulse width increases during positive slope condition & decreases under negative slope condition. Pulse width will be maximum at the +ve peak and minimum at the –ve peak of sinusoidal waveform. Record the observations.
7. Feed PWM waveform to the circuit of Fig.2 and observe the resulting demodulated waveform.

Observations:

S.No.	Control voltage (V_{P-P})	Output pulse width (m sec)



13(b). PULSE POSITION MODULATION & DEMODULATION

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Aim: To generate pulse position modulation and demodulation signals and to study the effect of amplitude of the modulating signal on output.

Apparatus required:

Name of the apparatus	Specifications/Range	Quantity
Resistors	3.9kΩ, 3kΩ, 10kΩ, 680kΩ	Each one
Capacitors	0.01μF, 60μF	2,1
Function Generator	1MHz	1
RPS	0-30v,1A	1
CRO	0-30MHz	1
IC 555	Operating tem :SE 555 -55°C to 125°C NE 555 0° to 70°C Supply voltage :+5V to +18V Timing :μSec to Hours Sink current :200mA Temperature stability :50 PPM/°C change in temp or 0-005% /°C.	1
CRO Probes	----	1

Theory:

In Pulse Position Modulation, both the pulse amplitude and pulse duration are held constant but the position of the pulse is varied in proportional to the sampled values of the message signal. Pulse time modulation is a class of signaling techniques that encodes the sample values of an analog signal on to the time axis of a digital signal and it is analogous to angle modulation techniques. The two main types of PTM are PWM and PPM. In PPM the analog sample value determines the position of a narrow pulse relative to the clocking time. In PPM rise time of pulse decides the channel bandwidth. It has low noise interference.

Circuit Diagram:

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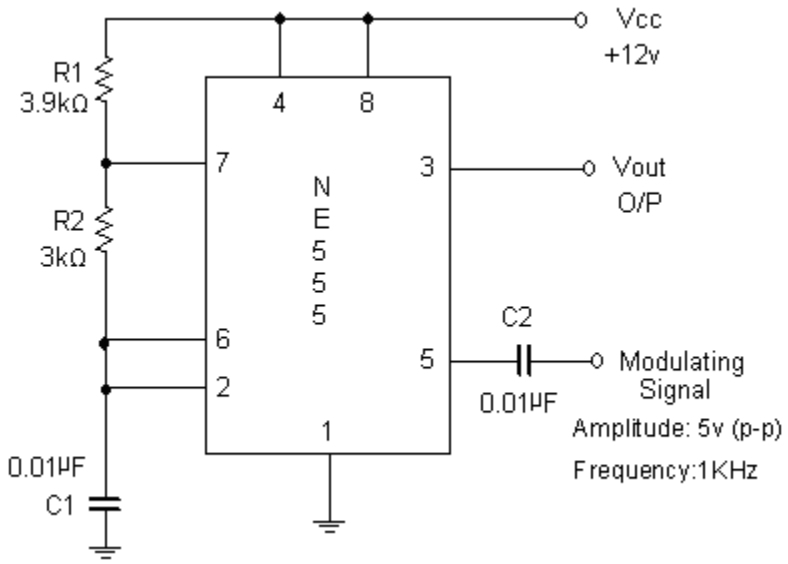

Fig: 1 Pulse Position Modulation Circuit

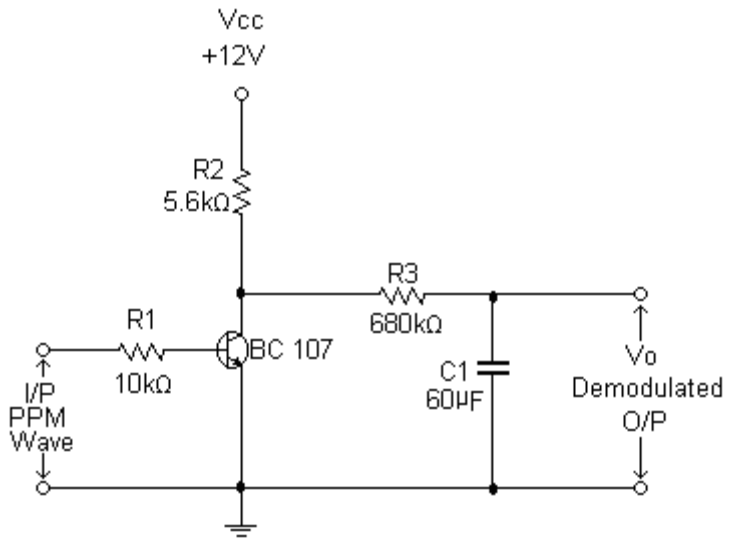

Fig: 2 Demodulation Circuit

Procedure:

1. Connect the circuit as per circuit diagram as shown in the fig 1.

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2. Observe the sample output at pin 3 and observe the position of the pulses on CRO and adjust the amplitude by slightly increasing the power supply. Also observe the frequency of pulse output.
3. Apply the modulating signal, sinusoidal signal of $2V_{(p-p)}$ (ac signal) 2v (p-p) to the control pin 5 using function generator.
4. Now by varying the amplitude of the modulating signal, note down the position of the pulses.
5. During the demodulation process, give the PPM signal as input to the demodulated circuit as shown in Fig.2.
6. Observe the o/p on CRO.
7. Plot the waveform.

Observations:

Modulating signal Amplitude(V_{p-p})	**Time period(ms)**		**Total Time period(ms)**
	Pulse width ON (ms)	**Pulse width OFF (ms)**	

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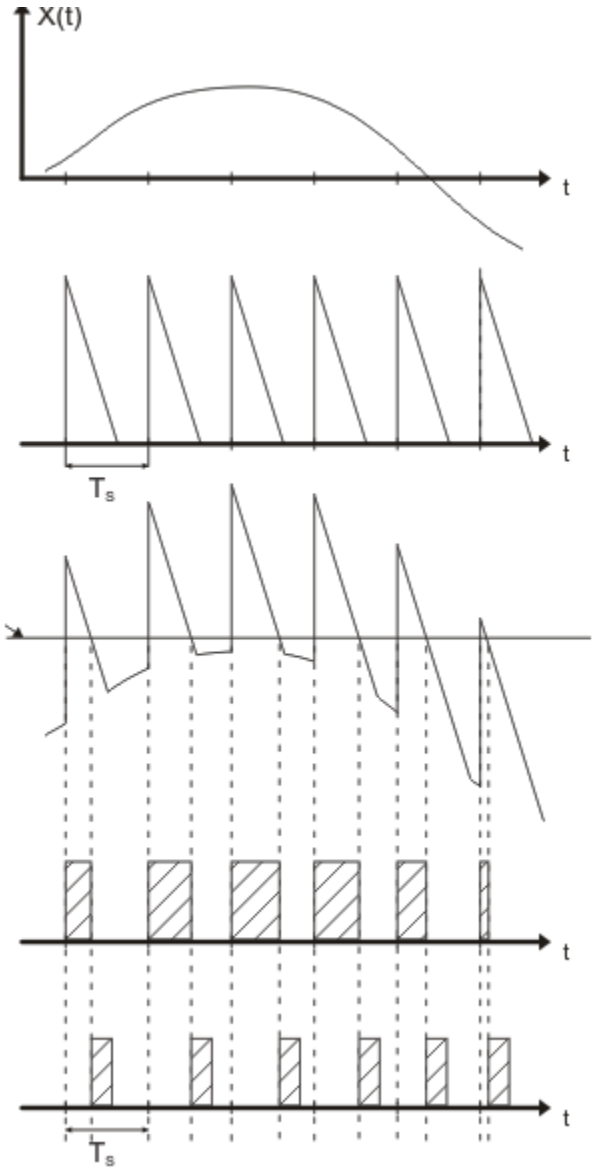

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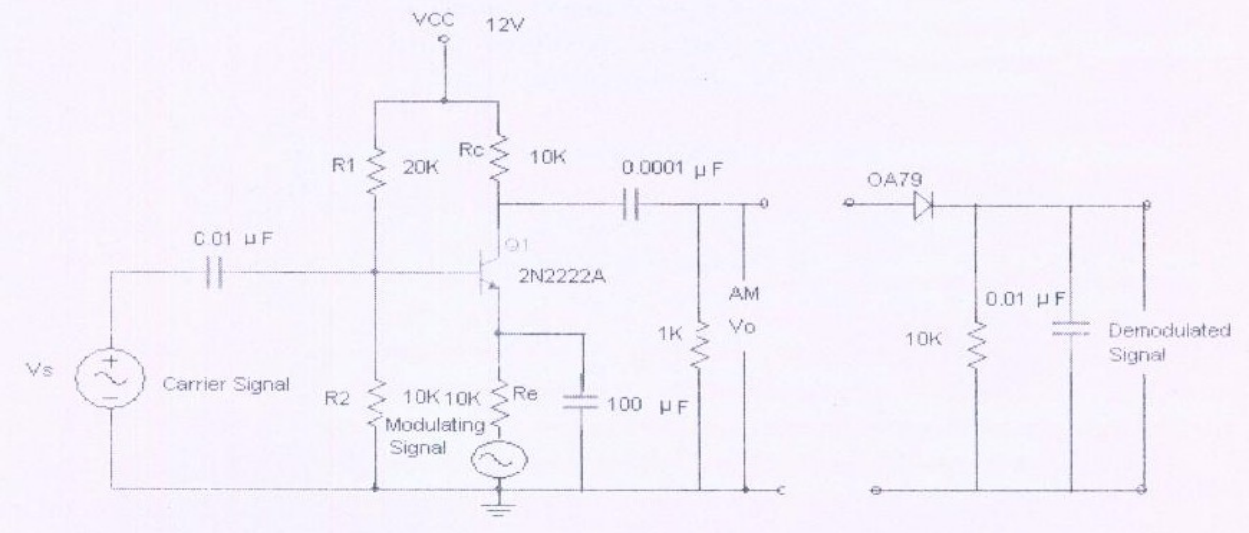
14. EFFECT OF NOISE ON COMMUNICATION CHANEL

AIM : Study the effect of the noise on communication channel

APPARATUS:

1. Double sideband AM Transmitter and Receiver Trainer Kit.
2. CRO
3. CRO probes
4. Connecting probes

CIRCUIT DIAGRAM:



PROCEDURE: MODULATION:

1. Ensure that the following initial conditions exist on the board.

   a). Audio input select switch in INT position.

   b). Mode switch in DSB position.

   c). Output Amplifier gain preset in fully clockwise position.

   d). speaker switch in OFF position.

2. Turn on power to ST2201 board.

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3. Turn the Audio oscillator blocks Amplitude preset to it's fully clockwise position and examine the blocks output (TP14) on CRO. This is the audio frequency sine wave which will be as output Modulating signal.

4. Turn the balance preset in Balanced Modulator and band pass filler circuit 1 block, to its fully clockwise position. It is the block that we will be used to perform double side band amplitude modulation.

5. Monitor the waveforms at TP1 and TP9 signal at TP1 is modulating signal and signal at TP9 is carrier signal to DSB-AM and observe the waveform at TP3 together with modulating signal, wave at TP3 is DSB-AM signal.

DEMODULATION

1. Ensure that the following initial conditions exist on the board ST220I.

   a) Tx output selector switch in antenna position.

   b) Audio amplifiers volume preset in fully counter clock wise position and speaker switch is in ON position.

2. Ensure that the following initial conditions exist on the board ST2202

   c) Rx input select switch in antenna position.

   d) RF amplifiers tuned circuit select switch in INT position.

   e) RF amplifiers gain preset in fully clock wise position.

   f) AGC switch in OUT position.

   g) Detector switch in product position.

   h) Audio amplifiers volume preset in fully counter clock wise position and speaker switch is in ON position. i) Beat frequency oscillator switch in ON position.

3) Transmit the DSB-AM wave to the ST2202 receiver by selecting The Tx output select switch in the ANT position.

4. Monitor the detected modulating signal ay TP37.Observe the Variations by varying the amplitude and frequency of the modulating signal in ST2201.

5. Observe the effect of noise which is created externally on Amplitude modulated and demodulated signals. Distortion in the modulating signals with noise.

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15 Design of Mixer

Aim: To design and obtain the characteristics of a mixer circuit.

Apparatus Required:

Name of the Component/Equipment	Specifications/Range	Quantity
Transistors (BC 107)	f_T = 300 MHz P_d = 1W I_c(max) = 100 mA	1
Resistors	1 KΩ , 6.8 KΩ, 10KΩ	1 each
Capacitor	0.01μF	1
Inductor	1mH	1
CRO	20MHZ	1
Function Generator	1MHz	1
Regulated Power Supply	0-30v, 1A	1

Theory:

The mixer is a nonlinear device having two sets of input terminals and one set of output terminals. Mixer will have several frequencies present in its output, including the difference between the two input frequencies and other harmonic components.

Circuit Diagram:

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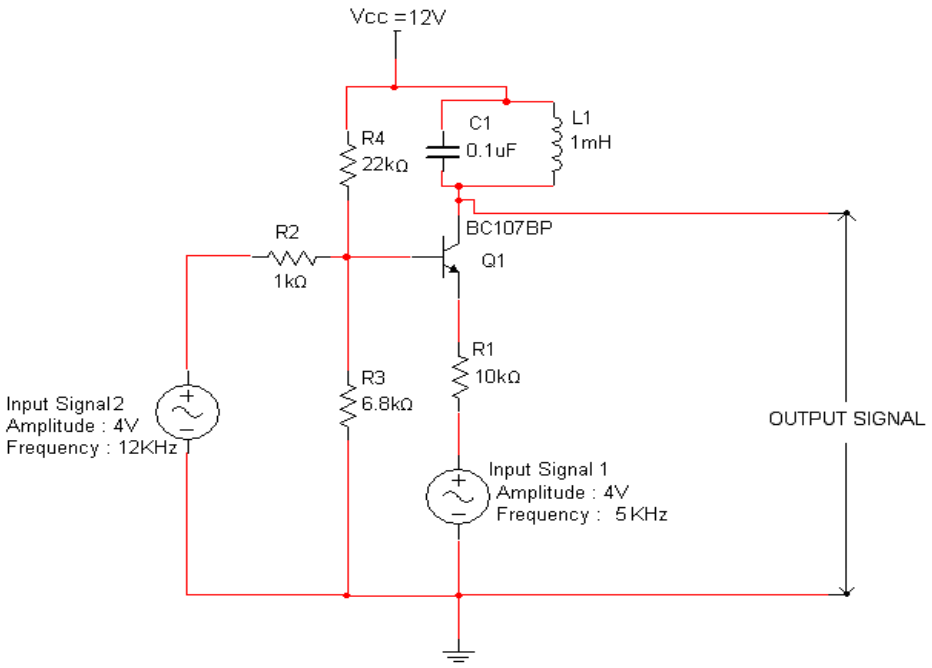

FIG.1. Mixer Circuit

Procedure:

1. Connect the circuit as per the circuit diagram as shown in Fig.1. Assume C=0.1μF and calculate value of L_1 using f= $\frac{1}{2\pi\sqrt{L_1 C_1}}$ where f=7KHz
2. Apply the input signals at the appropriate terminals in the circuit.
3. Note down the frequency of the output signal, which is same as difference frequency of given signals.

Sample readings:

Signal	Amplitude (Volts)	Frequency(KHz)
Input signal1	4	5
Input signal 2	4	12
Output signal	9	7

Waveforms:

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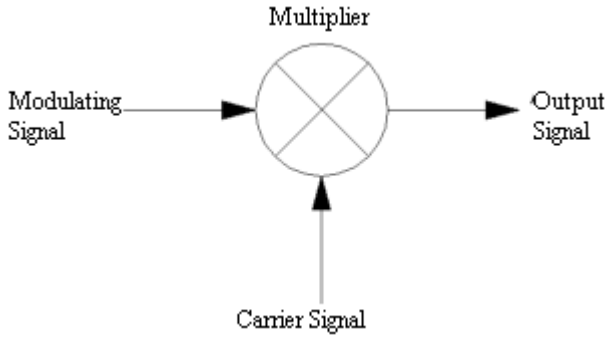

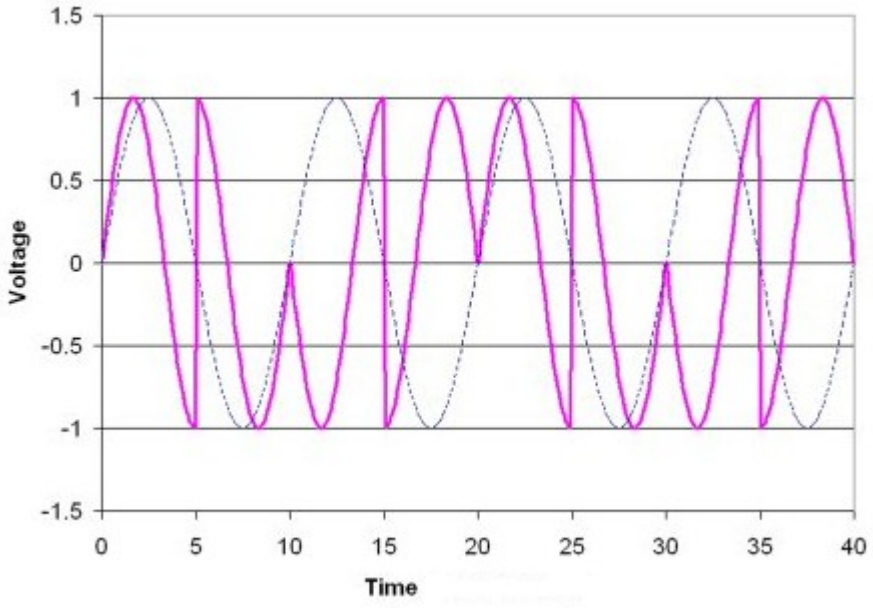

Precautions:

1.Check the connections before giving the supply

2.Observations should be done carefully